User Guide

SC9-TOCCATA • CompactPCI® Serial CPU Card

11th Generation XEON® W Processors
Tiger Lake H

Contents

About this Manual

This manual describes the technical aspects of the SC9-TOCCATA, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents	Author	Date
1	User Manual SC9-TOCCATA, english, preliminary edition (formal structure and some content), Text #10057, File: sc9_ug.wpd	jj	2022-03-29
2	Updated local PCI and SMB/I^2C Device Tables Updated section “Hardware Monitor NCT7491" Updated section “Board Control and Status Registers (BCSR)” Removed RM590E GPIO Table	gn	2022-04-14
3	Changed red OT front panel LED to HT (high temperature, yellow) Changed I225-IT NIC to I226-IT Added comment on future product VC1-TOCCATA to section PCI Express®	jj	21 April 2022
4	Added photos of CPU carrier card and mezzanine modules	jj	5 September 2022
5	Added AI Resources to table 'Feature Summary'	jj	4 October 2022
5.1	Added MTBF	gn/jj	26 January 2023
6	Added illustration TCSS (Type-C Subsystem)	gn/jj	16 February 2023
7	Added HWiNFO Diagnostics	gn/jj	17 March 2023
8	Added AirMax VSe® 25Gbps backplane connector information, added S83-P6 low profile mezzanine module	jj	12 April 2023
8.1	Modified F/P illustration according to moved LED positions PG/GP introduced with PCB Rev. 2	jj	25 August 2023
8.2	Updated F/P LED illustration introduced with PCB Rev. 2, added UEFI & ACPI release	jj	22 September 2023
8.3	Updated illustrations introduced with PCB Rev. 2: Component Orientation, PCB Dimensions	jj	27 November 2023
8.4	Table 'Feature Summary - Processor Characteristics': Junction temperature values precisely denoted as 'T_j' (not to confuse with board operating temperature conditions)	jj	4 December 2023
8.5	Table 'Feature Summary - Processor Characteristics': CPU base frequencies added in addition to turbo values	jj	7 December 2023

Related Documents

Related Information SC9-TOCCATA	
SC9-TOCCATA Home	www.ekf.com/s/sc9/sc9.html
SC9-TOCCATA Product Information	www.ekf.com/s/sc9/sc9_pi.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- XEON®, Core™: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Please note: If an EKF product has been labelled with this special sign according to ISO 7010 M002, please contact support@ekf.com for availability of additional documentation which may be important for proper usage.

Standards

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CompactPCI® Serial Specification, PICMG® CPCI-S.0	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version 1.4a, DisplayPort Alt Mode on USB Type-C	www.vesa.org
Ethernet	IEEE Std 802.3 2.5GBASE-T, 1000BASE-T, 100BASE-TX, 10BASE-T IEEE Std 1588 Precision Time Protocol	standards.ieee.org
HD Audio	High Definition Audio Specification	www.intel.com
eSPI	Intel Enhanced Serial Peripheral Interface Bus Interface Base Specification	www.intel.com
M.2	PCI Express M.2 Specification	www.pcisig.com
NVMe	NVM Express specification	www.nvmexpress.org
PCI Express®	PCI Express® Base Specification	www.pcisig.com
SATA	Serial ATA 3.0 & 3.1 Specification	www.sata-io.org
TPM	Trusted Platform Module 2.0	www.trustedcomputinggroup.org
UEFI	Unified Extensible Firmware Interface UEFI Specification UEFI Shell Specification ACPI Specification Version	www.uefi.org
USB	Universal Serial Bus Specification Type-C Cable and Connector Specification Type-C Locking Connector Specification Universal Serial Bus Power Delivery Specification	www.usb.org

General

The SC9-TOCCATA is a rich featured high performance 4HP/3U CompactPCI® Serial CPU board, equipped with an Intel® 11th Generation XEON® Processor (Tiger Lake H45 platform) for demanding industrial applications.

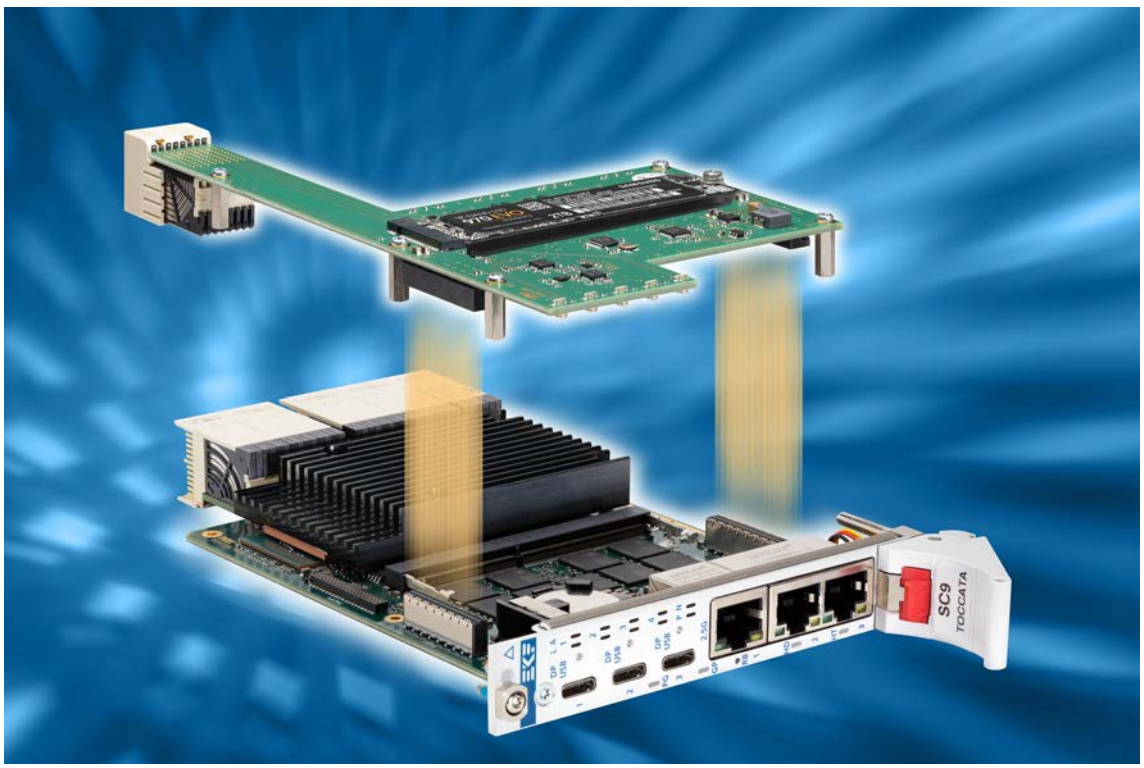
The SC9-TOCCATA front panel is provided with three 2.5Gbps Ethernet jacks for networking (2 x TCC/TSN capable) and three 10Gbps USB Type-C receptacles (DisplayPort Alternate Mode enabled) for versatile device and display attachment.

On-board mass-storage solutions are based on low profile mezzanine expansion cards, which accommodate up to two M.2 style SSD modules. One of the M.2 sockets is suitable for a fast NVMe (PCI Express® Gen4 x 4) module.

The SC9-TOCCATA is equipped with up to 64GB DDR4 ECC RAM. Up to 32GB memory-down are provided for rugged applications, and another 32GB are available via the DDR4 ECC SODIMM socket.

The 11th Generation XEON® and Core™ processors are accompanied by the RM590E mobile PCH, for a maximum of high speed I/O resources (e.g. PCI Express®, SATA, USB). Altogether with the processor, 25 PCIe® lanes in total are provided for backplane use, and another 8 lanes for local mezzanine expansion up to PCIe® Gen4 speed.

As an option, up to eight additional Gigabit Ethernet ports (either switch or NICs) are available via the backplane connector P6 by means of a mezzanine module.



Feature Summary

Feature Summary

General

- PICMG® CompactPCI® Serial (CPCI-S.0) CPU card
- Form factor single size Eurocard (board dimensions 100x160mm^2)
- Mounting height 3U
- Front panel width 4HP (8HP/12HP assembly with optional mezzanine side card)
- Front panel I/O connectors for typical system configuration (3 x 10Gbps USB Type-C DP Alt Mode, 3 x 2.5Gbps Ethernet RJ45)
- Backplane communication via PCI Express® up to Gen4, SATA 6G, USB 3.2, Gigabit Ethernet
- New AirMax VSe® backplane connectors up to 25Gb/s differential pair
- Local mezzanine expansion option, COTS and custom specific boards

Feature Summary

Processor Characteristics

- Intel® 11th Generation Mobile XEON® W or Core™ processor
- Tiger Lake H45 platform
- Up to 8-core, up to 3MB cache per core
- DDR4 3200 ECC RAM
- Gen 12 graphics, 4 displays up to 8k60
- TCC/TSN
- Extended temperature operation (CPU junction temperature range T_j up to -40°C to +100°C)
- Embedded & industrial use conditions
- 45/35W configurable TDP, 25W TDP
- BGA soldered for optimum reliability
- Mobile Intel® Series 500 PCH (RM590E IOTG)

- Intel® Xeon® W processors (Industrial Use Case *)
- Up to 8 cores, 24MB cache, 32EU, Intel® vPro™ eligible
- W-11865MRE | 8c 24M | 4.7GHz Turbo | 2.6GHz Base | 45/35W | 32EU 1350MHz | ECC | TCC/TSN | VPro | T_j -40°C to +100°C | SC9-650D-TOCCATA
- *W-11555MRE | 6c 12M | 4.5GHz Turbo | 2.6GHz Base | 45/35W | 32EU 1350MHz | ECC | TCC/TSN | VPro | T_j -40°C to +100°C*
- *W-11155MRE | 4c 8M | 4.4GHz Turbo | 2.4GHz Base | 45/35W | 16EU 1250MHz | ECC | TCC/TSN | T_j -40°C to +100°C*
- W-11865MLE | 8c 24M | 4.5GHz Turbo | 1.5GHz Base | 25W | 32EU 1350MHz | ECC | TCC/TSN | VPro | T_j 0°C to +100°C | SC9-440D-TOCCATA
- *W-11555MLE | 6c 12M | 4.4GHz Turbo | 1.9GHz Base | 25W | 32EU 1350MHz | ECC | TCC/TSN | VPro | T_j 0°C to +100°C*
- W-11155MLE | 4c 8M | 3.1GHz Turbo | 1.8GHz Base | 25W | 16EU 1250MHz | ECC | TCC/TSN | T_j 0°C to +100°C | SC9-340D-TOCCATA

  * disable core/graphics turbo for industrial use condition

- Intel® Core™ processors (Embedded Use Case)
- *i7-11850HE | 8c 24M | 4.7GHz Turbo | 2.6GHz Base | 45/35W | 32EU 1350MHz | VPro | T_j 0°C to +100°C*
- *i5-11500HE | 6c 12M | 4.5GHz Turbo | 2.6GHz Base | 45/35W | 32EU 1350MHz | VPro | T_j 0°C to +100°C*
- *i3-11100HE | 4c 8M | 4.4GHz Turbo | 2.4GHz Base | 45/35W | 16EU 1250MHz | T_j 0°C to +100°C*
- 6600HE | 2c 8M | 2.6GHz | 35W | 16EU 1100MHz | T_j 0°C to +100°C | SC9-140D-TOCCATA
- *6600HLE | 2c 8M | 2.1GHz | 25W | 16EU 1100MHz | T_j 0°C to +100°C*

Feature Summary

AI (Artificial Intelligence) Resources

- DL Boost - set of instructions to accelerate AI workloads
- AVX512 - Advanced Vector Extensions & VNNI - Vector Neural Network Instructions - X86 instruction set which is designed to accelerate convolutional neural network for INT8 inference, helps accelerate workloads like image recognition
- GNA - Gaussian & Neural Accelerator - a low-power neural coprocessor for continuous inference at the edge, designated for offloading workloads including but not limited to noise reduction or speech recognition, saves power and frees CPU resources
- Intel® OpenVINO™ (Open Visual Inference and Neural network Optimization) toolkit 2022 - deploy high-performance, deep learning inference
- Intel® Edge Software Hub - edge compution software and packages
- Intel® DevCloud for the Edge - allows you to actively prototype and experiment with AI workloads for computer vision

Firmware

- Phoenix® UEFI (Unified Extensible Firmware Interface) V2.7
- Phoenix SCT (SecureCore Technology) Release V4.3.0
- ACPI V6.1
- Fully customizable by EKF
- Secure Boot and Measured Boot supported - meeting all demands as specified by Microsoft®
- Windows®, Linux and other (RT)OS supported
- Intel® AMT vPro® supported (disabled by default, must be enabled via BIOS setup)

Main Memory

- Integrated memory controller up to 64GB DDR4 3200 with hardware ECC *
- DDR4 +ECC soldered memory up to 32GB (ultra rugged basic memory)
- DDR4 +ECC SO-DIMM memory module socket up to 32GB (memory expansion option)
- Total memory encryption

* ECC with XEON® processor SKUs (industrial use)

Feature Summary

Graphics

- Integrated X^{e} Gen 12 graphics engine, 4 displays
- Up to 32EU
- Codec support HEVC/SCC/VP9/AV1
- HDR support power optimized
- Decode up to 8k60:
  - 2x 4k60 8b 4:2:0 AVC
  - 5k60 12b 4:2:2/4:4:4 HEVC/VP9/SCC
  - 8k60 12b 4:2:0 HEVC/VP9/SCC
  - 4k60 10b 4:2:0 AV1
- Encode up to 8k30:
  - 2x 4k60 8b 4:2:0 AVC
  - 5k60 10b 4:4:4 HEVC/VP9/SCC
  - 8k30 10b 4:2:0 HEVC/VP9/SCC
  - 2x 4k HEVC encode speed
- Up to 4 displays supported:
  - 1 Display: 8k60 HDR
  - 2 Displays: 8k60 SDR or 4k120 HDR + 5k120 HDR
  - 3 Displays: 4k60 HDR
  - 4 Displays: 4k60 HDR
- DisplayPort DP1.4a HBR3
- Multi-Stream Transport (MST) - display daisy chaining
- Integrated DP Alt Mode MUX
- Integrated audio

- Display front panel options:
- 3 x Type-C connectors for either DisplayPort and USB usage
- 4th DisplayPort optional via Type-C connector on low profile mezzanine card S40 or S48

Feature Summary

Networking

- Up to 11 Ethernet networking interfaces in total
- 3 x Front 2.5GBASE-T RJ45 - 3 x Intel® I226-IT NIC
- 2.5GBASE-T, 1000BASE-T, 100BASE-TX, 10BASE-T connections
- RJ45 Front port 1 - Intel® I226-IT, Intel® vPro®/AMT (Wake on LAN)
- RJ45 Front port 2 - Intel® I226-IT, TCC/TSN capable, PPS/PPM Signaling
- RJ45 Front port 3 - Intel® I226-IT, TCC/TSN capable
- Integrated TCC/TSN controller for front ports 2 & 3 (RM590E PCH) - Real Time networking
- TSN Precision time protocol (Time-Sensitive-Networking) as required e.g. for OPC UA and OpenAvnu
- Enables ultra-reliable low-latency communication (URLLC)
- Intel® Time Coordinated Computing (Intel® TCC) for time synchronisation and timeliness
- Option 8 x 1000BASE-T backplane w. S80-P6 mezzanine module - Marvell® Peridot switch
- Option 4 x 1000BASE-T backplane w. S82-P6 mezzanine module - 4 x Intel® I210-IT NIC
- Option 4 x 2.5GBASE-T backplane w. S83-P6 mezzanine module - 4 x Intel® I226-IT NIC
- Option 4 x 2.5GBASE-T RJ45 front w. SCJ-VEENA side card - 4 x Intel® I226-IT NIC (8HP assembly)
- Option 4 x 1000BASE-T M12-X front w. SCL-RHYTHM side card - 4 x Intel® I210-IT NIC (8HP assembly)
- Option RJ45 port 1 jack (vPro®/AMT) replacement by M12-X connector w. S02-M12 mezzanine (8HP)

Security

- Total memory encryption - hardware based
- ROP attack prevention - hardware based protection against browser malware attacks
- Advanced Crypto Key protection - hardware based

- Trusted Platform Module SLM9670
- TPM 2.0 for highest level of certified platform protection
- Infineon Optiga™ cryptographic processor
- Conforming to TCG 2.0 specification

Front Panel I/O (4HP)

- 3 x 2.5Gbps Ethernet RJ45 receptacles
- 2.5GBASE-T, 1000BASE-T, 100BASE-TX, 10BASE-Te
- Intel® vPro®/AMT supported (port 1 RJ45 connector - must be enabled via BIOS settings)
- Port 2 & 3 TCC/TSN enabled

- 3 x 10Gbps USB Type-C receptacles DisplayPort Alt Mode
- USB and/or DisplayPort usage
- USB 3.2 Gen 2x1 (formerly USB 3.1 Gen2) SuperSpeed+ 10Gbps
- USB-PD downstream facing ports 5V/3A (Infineon CYPD5225 EZ-PD™ CCG5 controller)
- DisplayPort 1.4
- Additional Type-C front I/O with low profile mezzanine e.g. S40 or S48

Feature Summary

Front Panel I/O (8/12HP)

- Variety of side cards available, common front panel 8HP/12HP with CPU card
- For backplanes with system slot right aligned
- Various I/O ports e.g. UART, Audio, RJ45 Ethernet, M12-X Ethernet, Wireless (SMA)
- Custom specific front panel and side card design

CompactPCI® Serial Backplane Resources

- PICMG® CPCI-S.0 CPU card & system slot controller
- 16 x PCIe Gen4 [1] 16GT/s (2 links x8 for two fat pipe slots, derived directly from the Xeon® or Core™ CPU)
- 9 x PCIe Gen3 8GT/s (1 link x4, 5 links x1 for peripheral slots, derived from the PCH)
- 5 x SATA 6G (from the PCH)
- 8 x USB3 [2] (from the PCH)
- Option 8 x Gigabit Ethernet Marvell 88E6390 switch (S80-P6 low profile mezzanine expansion card)
- Option 4 x Gigabit Ethernet Intel® I210-IT NIC (S82-P6 low profile mezzanine expansion card)
- Option 4 x 2.5Gigabit Ethernet Intel® I226-IT NIC (S83-P6 low profile mezzanine expansion card)

- New backplane connectors AirMax VSe® up to 25Gbps per differential pair according to CompactPCI® Serial Rev. 3.0 (backward compatible to backplanes with AirMax VS® 12.5Gbps)
- 4HP CPU card front panel width when the adjacent board to the right is equipped with legacy AirMax VS® connectors (e.g. peripheral cards according to the CompactPCI® Serial R2.0 connector specification)
- 5HP CPU card front panel width and backplane slot pitch required when the adjacent board to the right is also equipped with the new AirMax VSe® connectors (e.g. multi CPU card system), will be introduced with CompactPCI® Serial R4.0

[1] The CPU is PCIe® Gen4 capable on these links (specified with CompactPCI® Serial R3.0)
[2] USB 3.2 Gen 2x1 SuperSpeed+ 10Gbps

Feature Summary

Local Expansion & Mezzanine Mass Storage Options

- Mezzanine side card connectors for optional local expansion
- Low profile mezzanine modules available (4HP front panel)
- Side cards available (8HP F/P assembly)
- HSE1 - PCIe Gen4 x4, 1 x USB3 10Gbps & 2 x USB2
- HSE2 - PCIe Gen3 x4 (configurable also 2x2, 4x1), 4th DisplayPort
- EXP - Legacy interface (eSPI, Audio, UART, I2C, GPIO)

- 4HP Low profile mezzanine module preferred options:
- S20-NVME Mezzanine module - M.2 2280 NVME SSD socket, 1 x Type-C USB F/P connector
- S40-NVME Mezzanine module - 1 x M.2 2280 NVME SSD socket, 1 x M.2 2280 SATA SSD socket, 2 x Type-C USB F/P connectors (1 connector enabled for DisplayPort alternate mode)
- S42-MC Mezzanine module - M.2 2280 NVME SSD socket, 2 x PCIe® Mini Card sockets
- S48-SSD Mezzanine module - 1 x M.2 2280 PCIe® x4 Gen4 SSD socket, 1 x M.2 2280 PCIe® x4 Gen3 SSD socket, Type-C USB F/P connector (enabled for DisplayPort alternate mode - 4th display)
- S80-P6 Mezzanine module - M.2 2280 NVMe SSD socket, 8 x Gigabit Ethernet via P6 backplane connector (switch based solution)
- S82-P6 Mezzanine module - M.2 NVMe SSD socket, 4 x GbE NIC via P6 backplane connector
- S83-P6 Mezzanine module - M.2 NVMe SSD socket, 4 x 2.5GbE NIC via P6 backplane connector
- Custom specific storage & I/O module design

- 8HP Mezzanine side card options:
- SCJ-VEENA Short side card - M.2 2280 NVMe SSD socket, 4 x 2.5GbE NIC, front panel RJ45, USB3
- SCL-RHYTHM Short side card - M.2 2280 NVMe SSD socket, 4 x GbE NIC, front panel M12-X
- SCZ-NVM - M.2 22110 NVMe SSD socket, quad UART, DisplayPort & USB3 connectors
- S02-M12 - RJ45 port 1 (vPro®/AMT) replacement by M12-X connector (top or bottom mount)
- Custom specific side card design - I/O and storage

- Backplane Coupler:
- SCX-PCIE - M.2 2280 NVMe/SATA SSD socket, PCIe® Mini Card socket, 3 x USB3, 3 x GbE RJ45 connectors, coupler for secondary CompactPCI® Serial backplane
- ECX-PCIE - Front I/O same as SCX, coupler for CompactPCI® Express secondary backplane

RT OS Board Support Packages

- Available on request

Applications

- High performance industrial and embedded computing, for x86 based software
- Automation, process control, test systems, demanding applications
- Edge computing, AI deep learning

Feature Summary

Environmental & Regulatory

- Suitable e.g. for industrial, transportation & instrumentation applications
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Long term availability
- Rugged solution
- Coating, sealing, underfilling on request
- Lifetime application support
- RoHS compliant
- Operating temperature 0°C to +70°C
- Operating temperature -40°C to +85°C (industrial temperature range) on request
- Storage temperature -40°C to +85°C, max. gradient 5°C/min
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 20.2 years (MIL-HDBK-217F, SN29500 @+40°C)
- EC Regulatory EN55035, EN55032, EN62368-1 (CE)

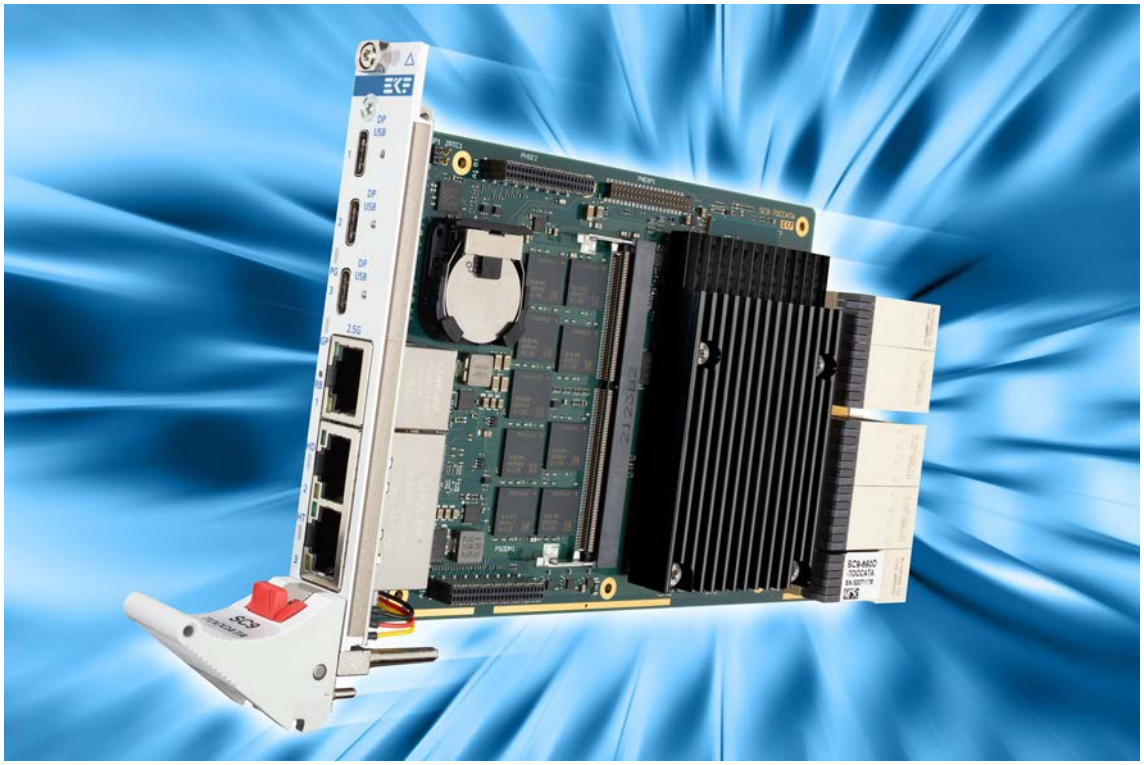
all items may be subject to technical changes w/o further notice

CompactPCI® Serial

While mechanically compliant to CompactPCI® Classic, CompactPCI® Serial (PICMG® CPCIS.0) defines a well established card slot system, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. Up to 6 high-speed backplane connectors P1 - P6 are provided on a system slot controller such as the SC9-TOCCATA, which can be considered as a root hub with respect to most signal lines. A passive backplane is used for distribution of a defined subset of I/O channels from the system slot to each of up to eight peripheral slots in a CompactPCI® Serial system.

Most CompactPCI® Serial peripheral slot cards require only the backplane connector P1, which comprises PCIe®, SATA and USB signals, resulting in a concise and inexpensive peripheral board design. More powerful peripheral cards profit from two so called Fat Pipe slots (PCIe® x 8).

The SC9-TOCCATA is a native CompactPCI® Serial CPU card, suitable for usage in a pure CPCI Serial environment. Due to its generous backplane capabilities (25 x PCI Express® up to Gen4, 8 x USB3, 5 x SATA 6G, up to 8 x GbE), very powerful industrial systems can be built.



Mezzanine Expansion

The SC9-TOCCATA is equipped with a set of high-speed local expansion interface connectors, which can be optionally used to attach either a low profile mezzanine module (fits into the 4HP front panel envelope) or a side card for an 8HP or even 12HP assembly in total.

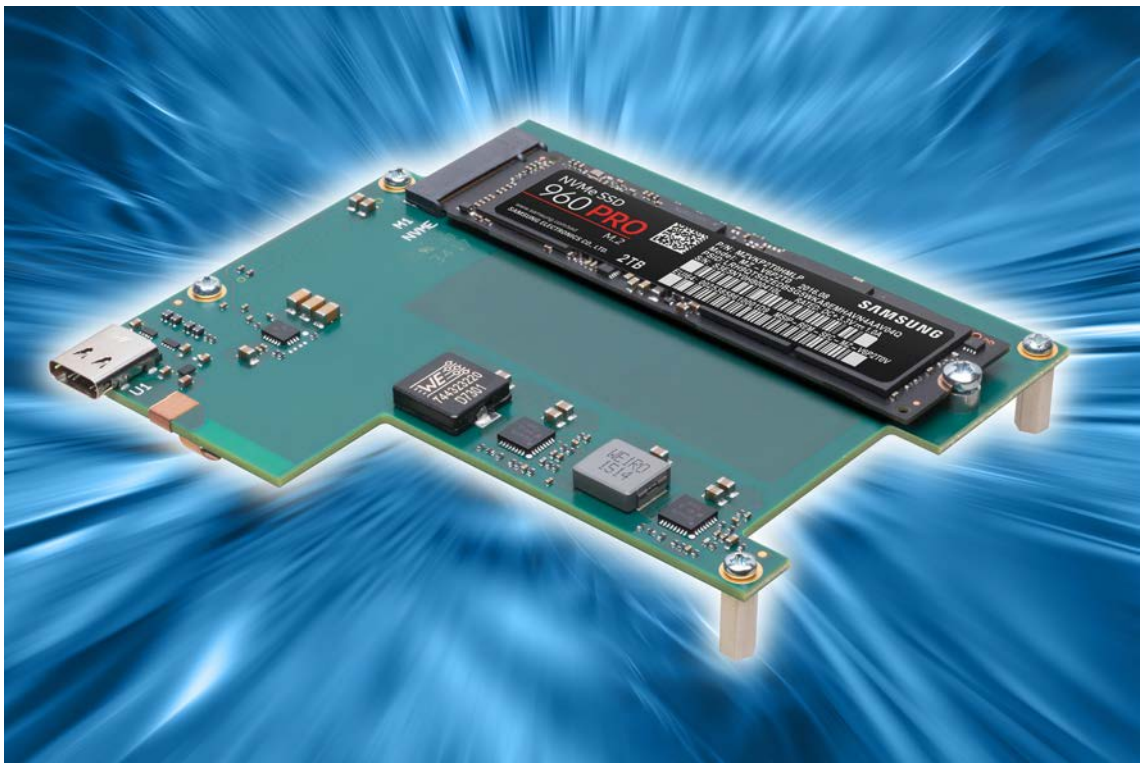
The connectors HSE1 and HSE2 are high speed connectors, as required for PCI Express® Gen4 and USB3 10Gbps. The socket EXP is used as a legacy interface (e.g. HD Audio, UART) and not required for many mezzanine modules. All mezzanine connectors allow board-to-board heights of 10.0mm (S20, S40, S48), 10.8mm (S80, S82), and 18.7mm (e.g. SCJ, SCL side cards 8HP assembly).

HSE1 is assigned to a PCIe® Gen4 x4 link, derived directly from the CPU. On a 4HP low profile mezzanine module or 8HP side card this link is wired to a fast Gen3 or Gen4 NVMe SSD housed in an M.2 socket, typically used as boot device and general mass storage. In addition, HSE1 brings a 10Gbps USB3 port, often used for additional front I/O.

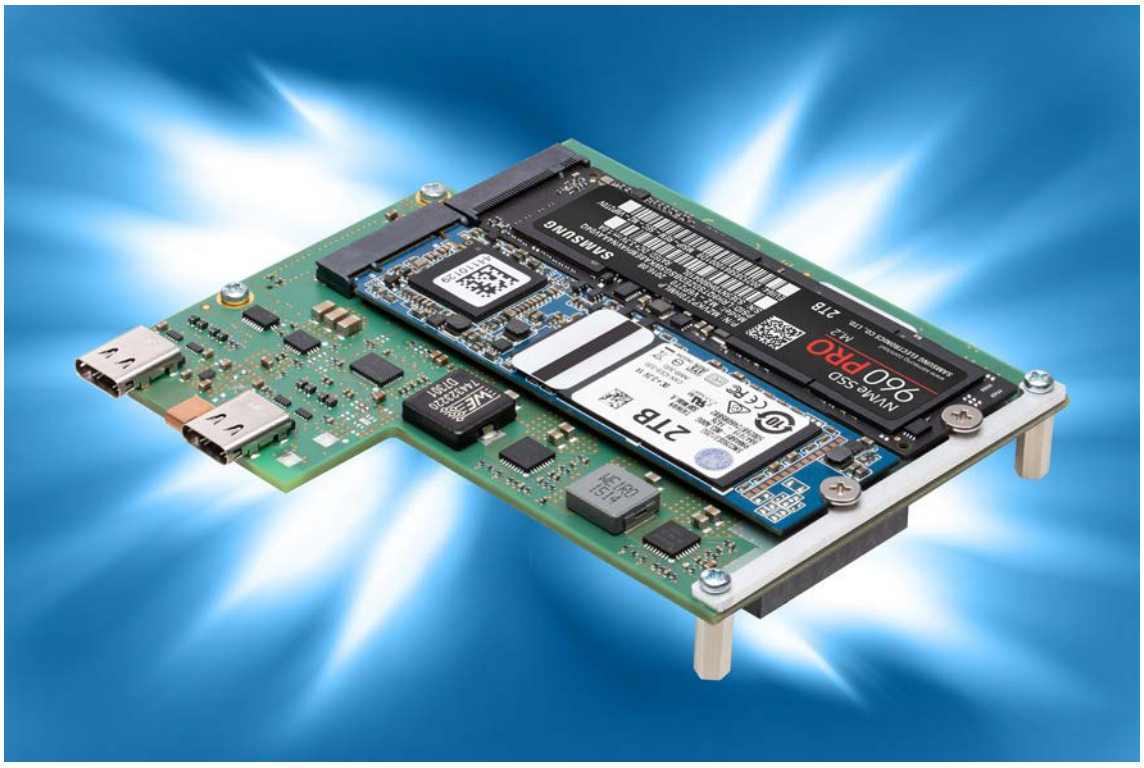
HSE2 provides another four PCIe® Gen3 lanes, configurable for versatile link width and combinations, and in addition a 4th DisplayPort video output. Some mezzanine modules such as the S20 get along with the HSE1 connector alone, others such as S40, S48 or S80 depend on both HSE1 and HSE2 for full functionality.

Related Information Mezzanine Connectors

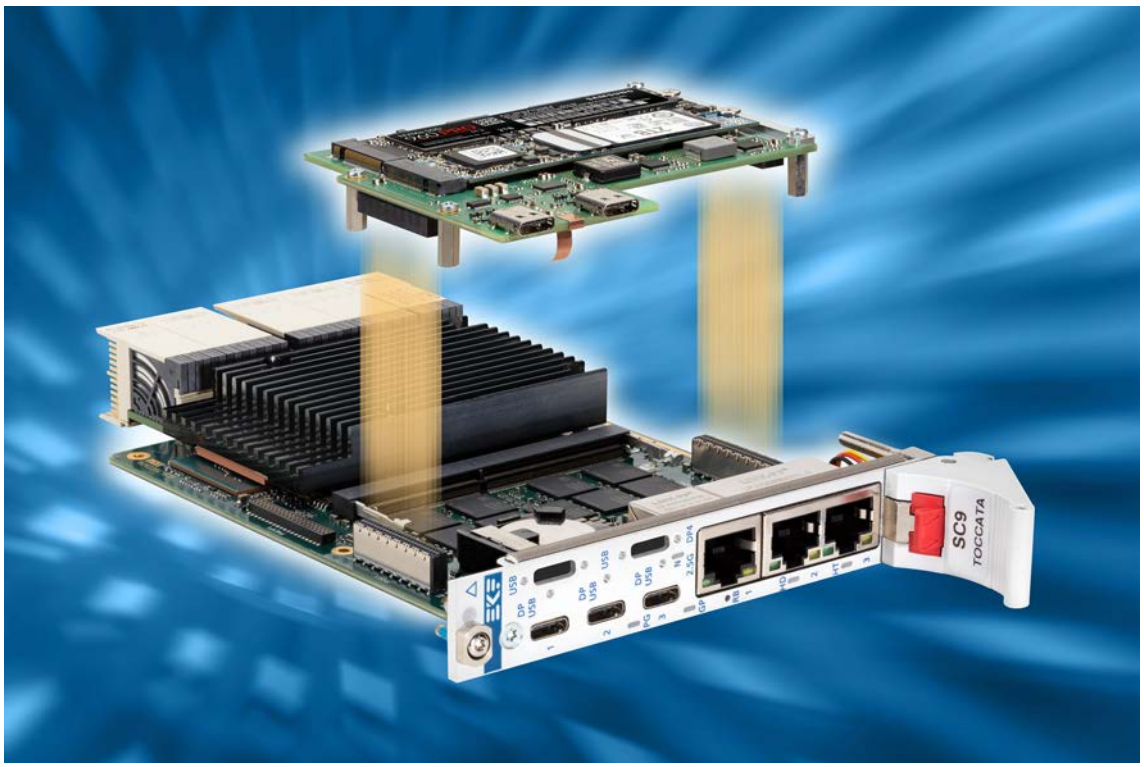
https://www.ekf.com/s/mezzanine_connectors.pdf



S20-NVME Low Profile Mezzanine Module

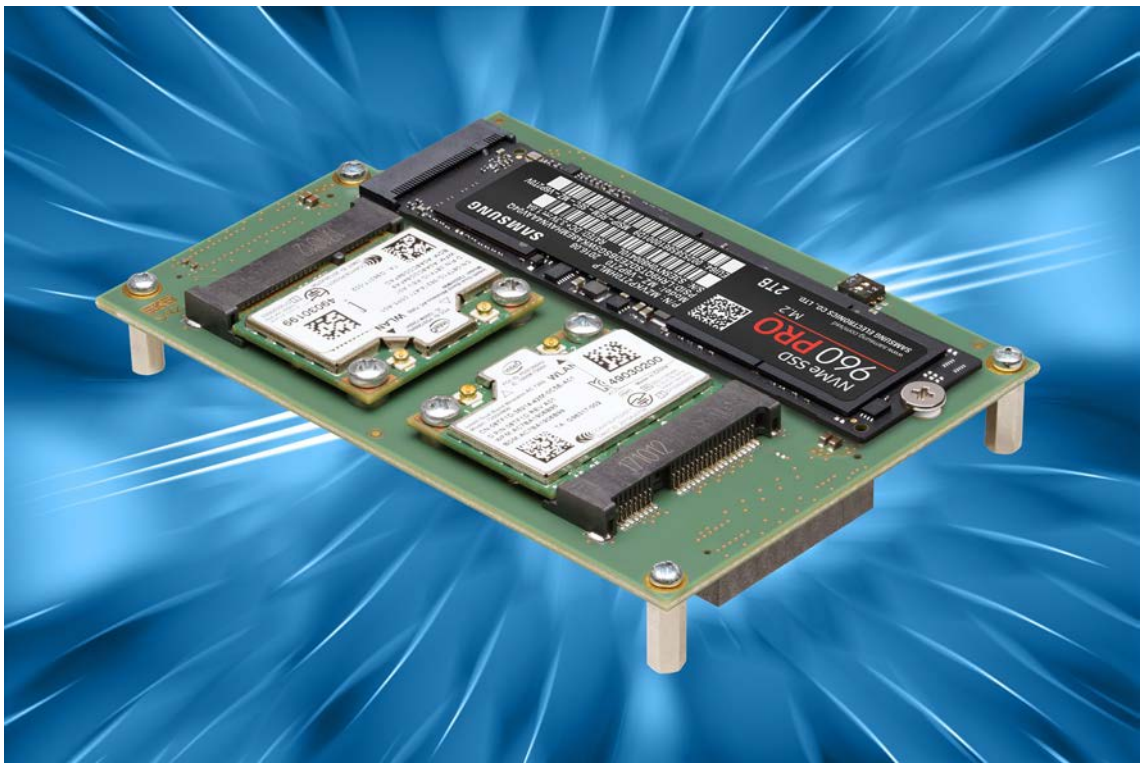


S40-NVME Low Profile Mezzanine Module

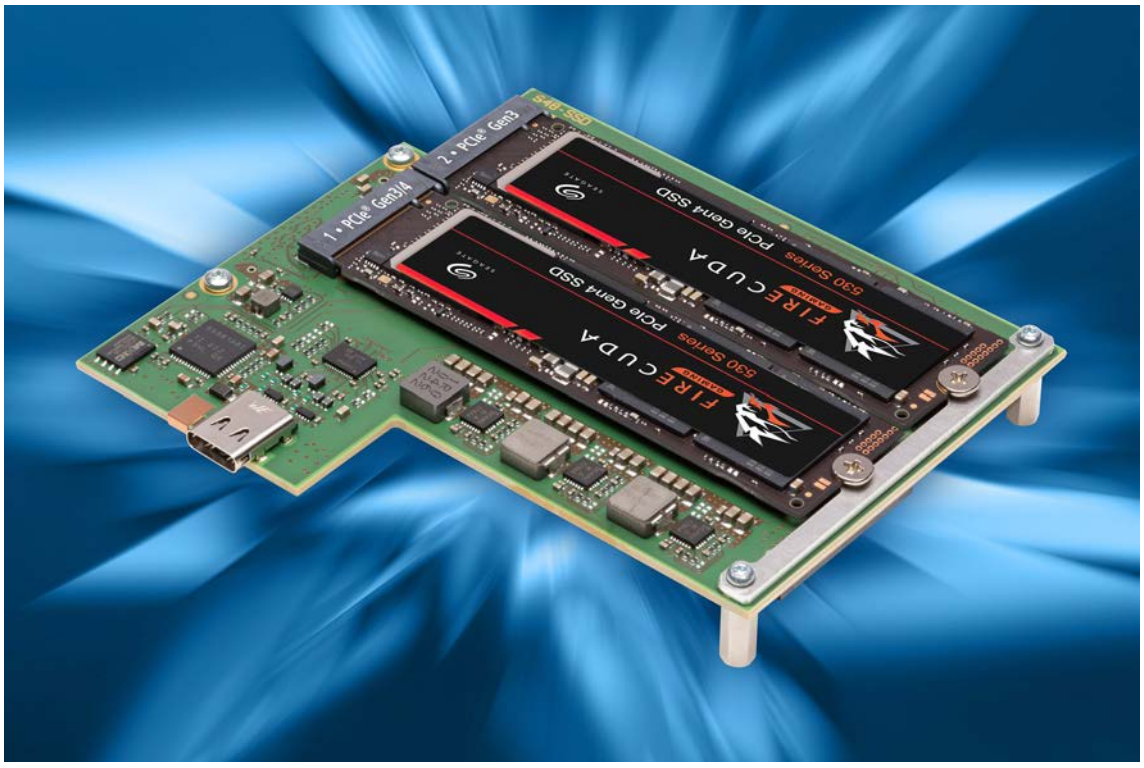


SC9 w, S40

SC9 w. S40



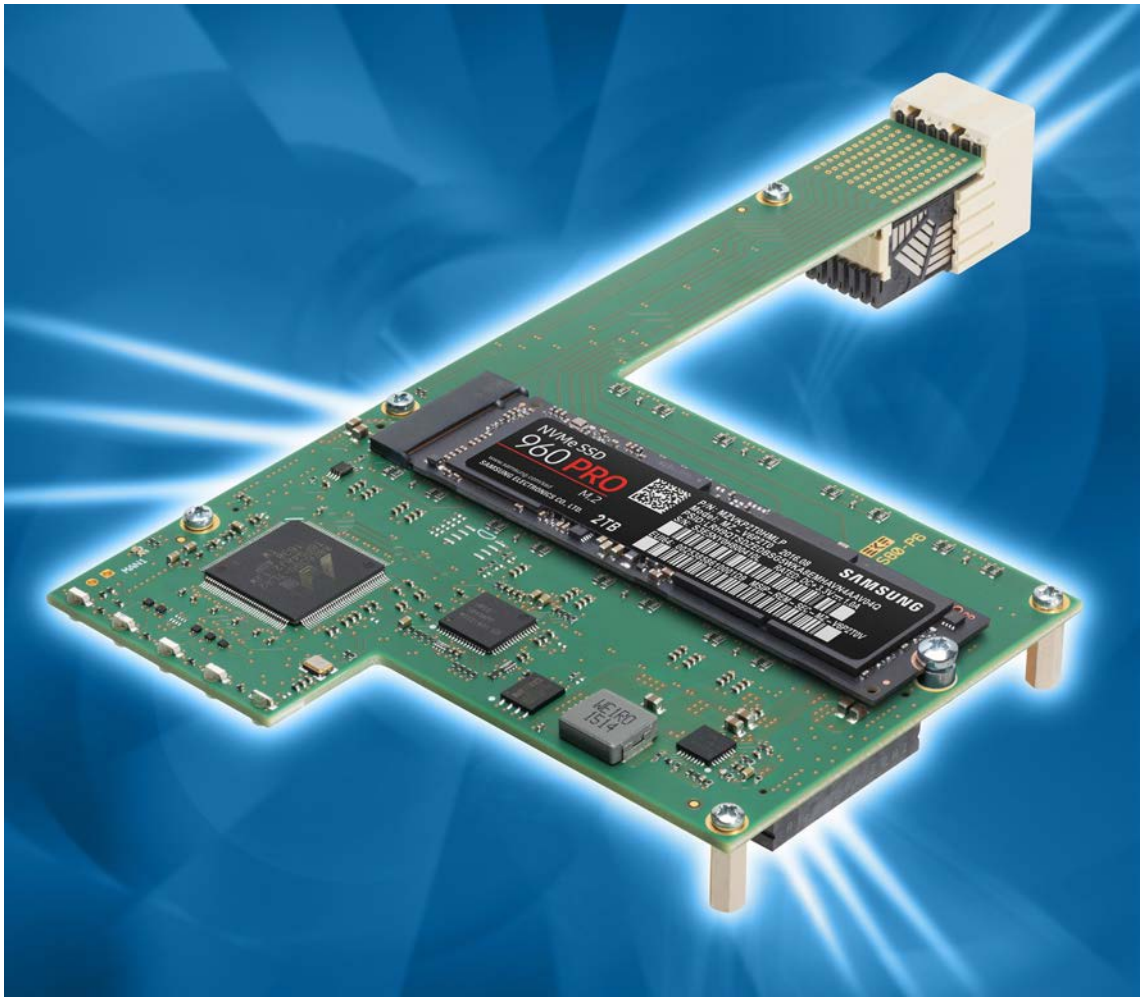
S42-MC Low Profile Mezzanine Module



S48-SSD Low Profile Mezzanine Module

SC9 w. S48

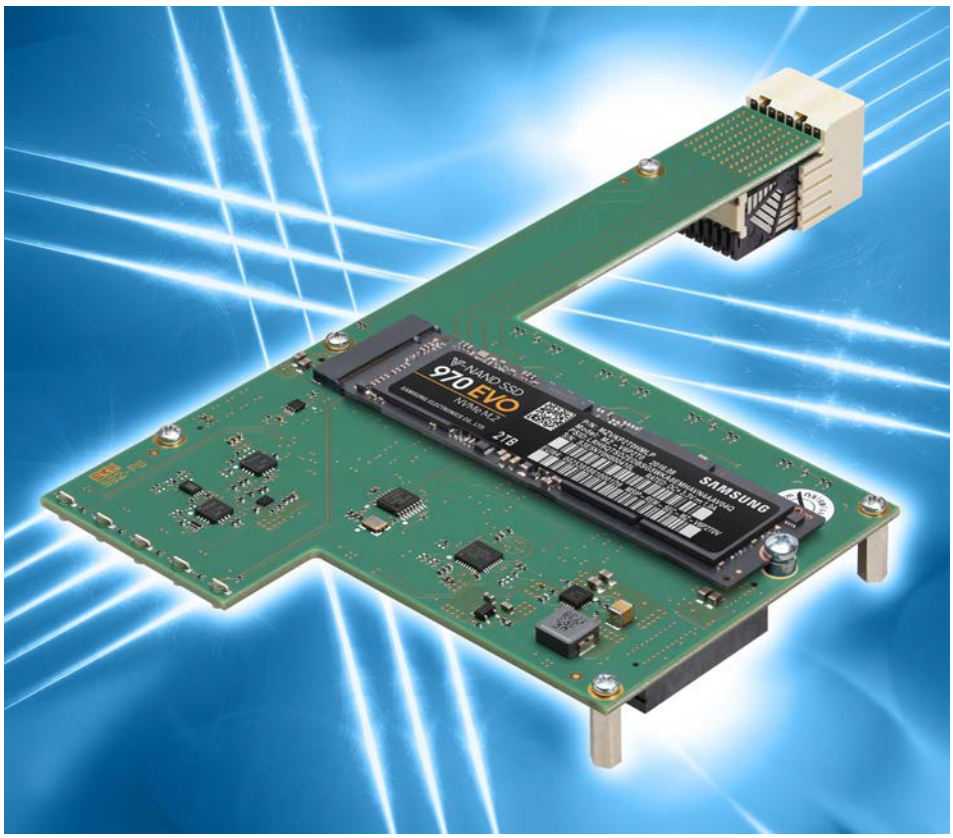
SC9 w. S48



S80-P6 Low Profile Mezzanine Module

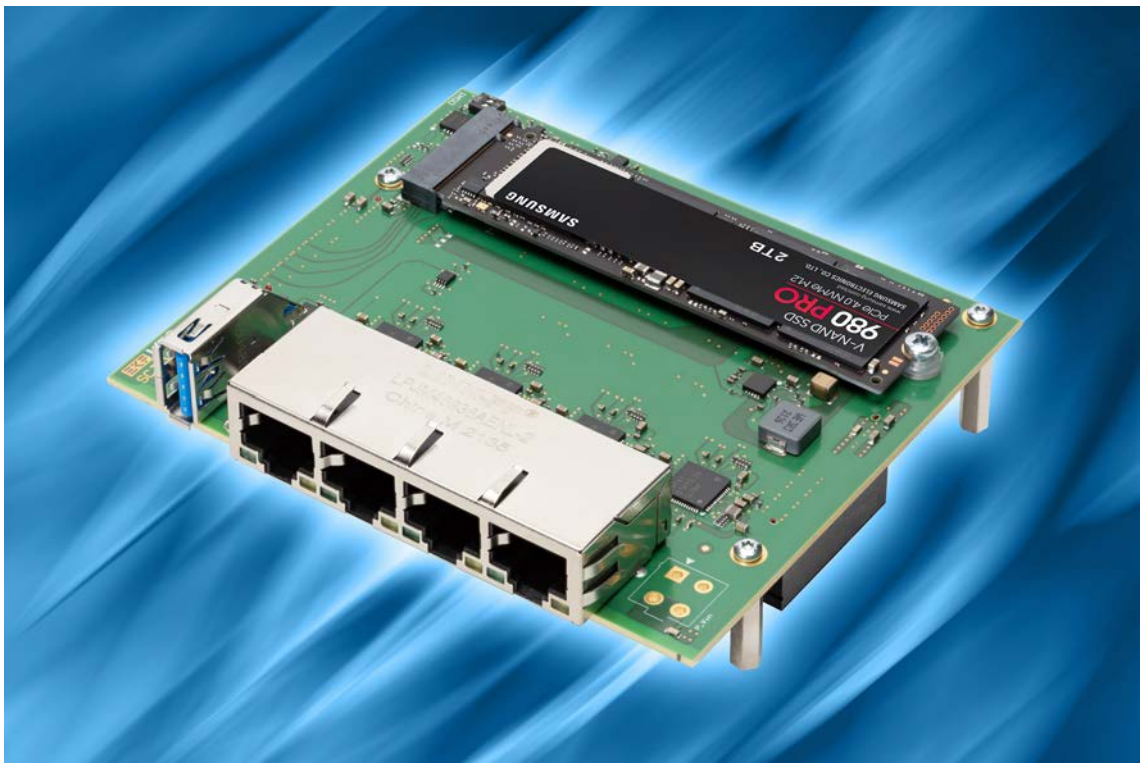
SC9 w. S80

SC9 w. S80



S82-P6 Low Profile Mezzanine Module

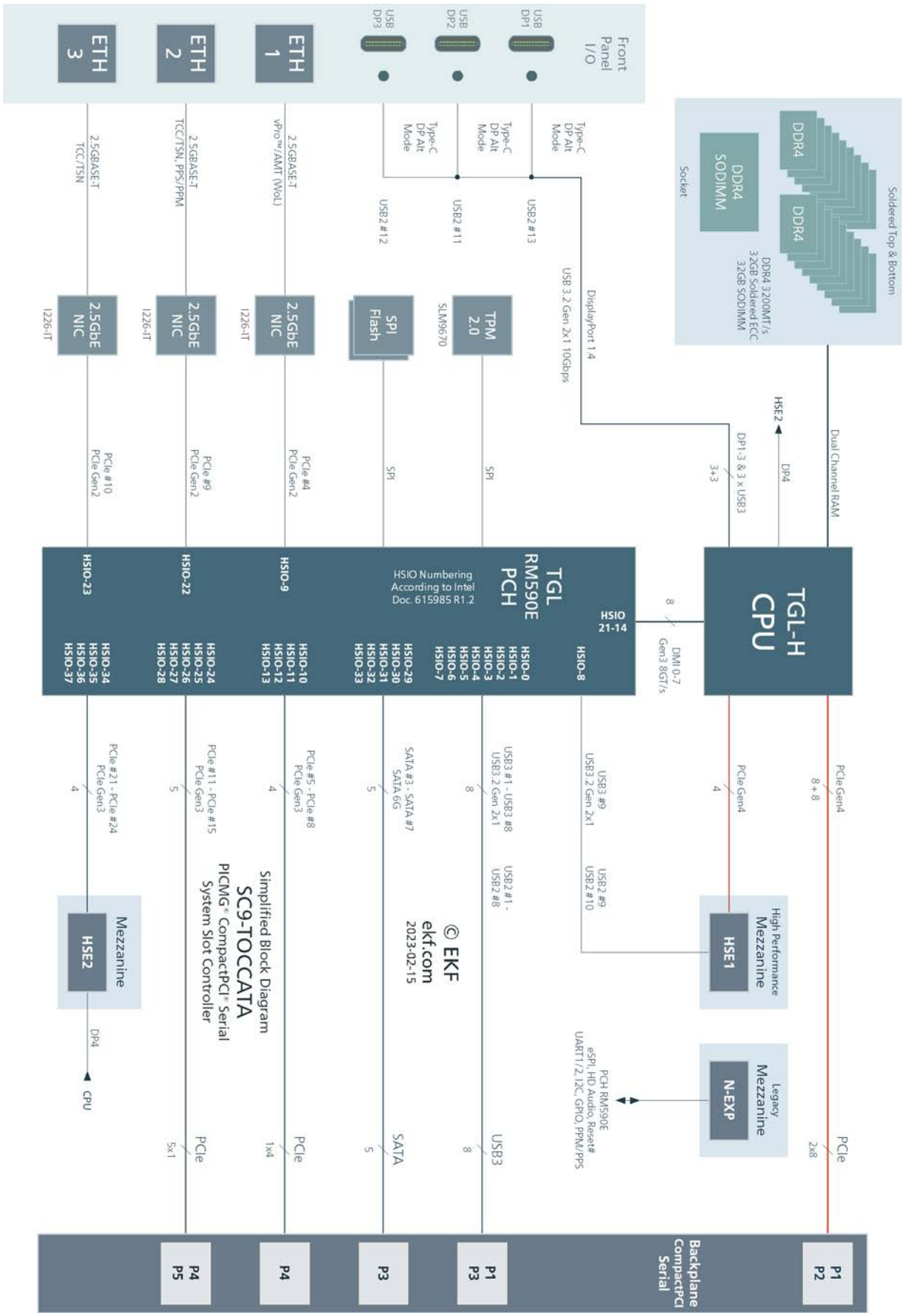
SCJ-VEENA 8HP Assembly



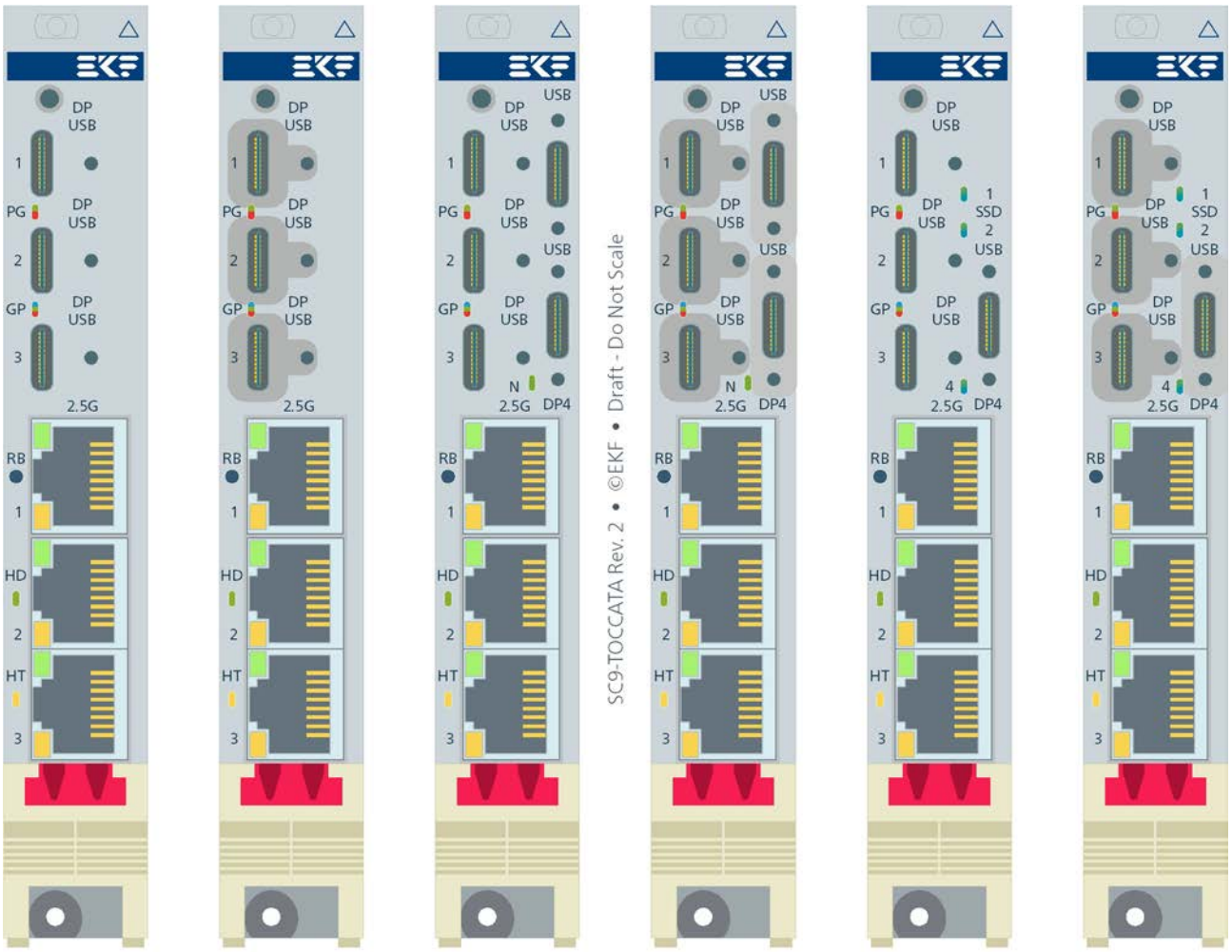
SCL-RHYTHM 8HP Assembly

SCZ-NVM 8HP/12HP Assembly

Block Diagram

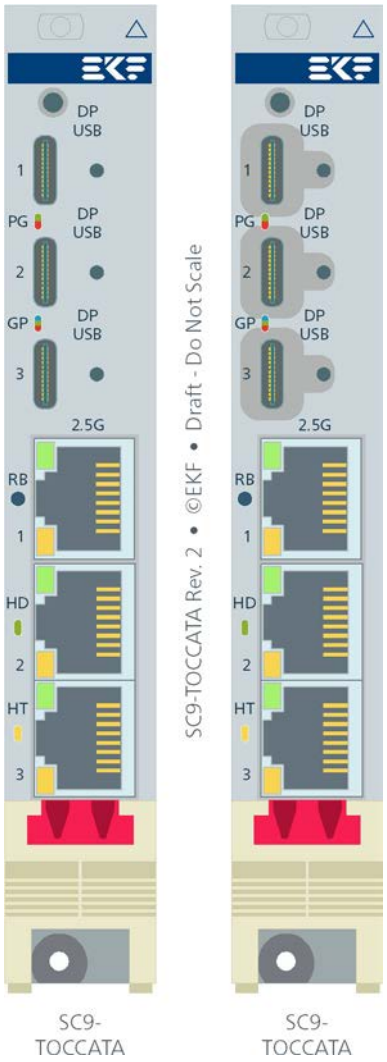


Front Panel


DP
USB
1
PG
2
GP
3
2.5G
RB
HD
HT
USB
N
DP4
1
SSD
2
4
SC9-TOCCATA Rev. 2 • ©EKF • Draft - Do Not Scale
SC9-
TOCCATA
SC9-
TOCCATA
SC9- w. S40
TOCCATA
SC9- w. S40
TOCCATA
SC9- w. S48
TOCCATA
SC9- w. S48
TOCCATA

Front Panel Connectors

USB/DP 1-3	Type-C USB 3.2 Gen 2x1 10Gbps & DisplayPort 1.4 Alternate Mode Processor connected ports USB-PD downstream facing ports, V_{BUS} 5V up to 3A (maximum power not available concurrently on any port) Front pane w. threaded M2x0.4 holes optionally available for screw locked cable assemblies (single screw USB Type-C locking plug)
Ethernet 1-3	RJ45 2.5GBASE-T via I226-IT NICs (1000BASE-T, 100BASE-TX, 10BASE-T) 1 - vPro™/AMT (WoL) capable 2 - TCC/TSN, PPS/PPM 3 - TCC/TSN

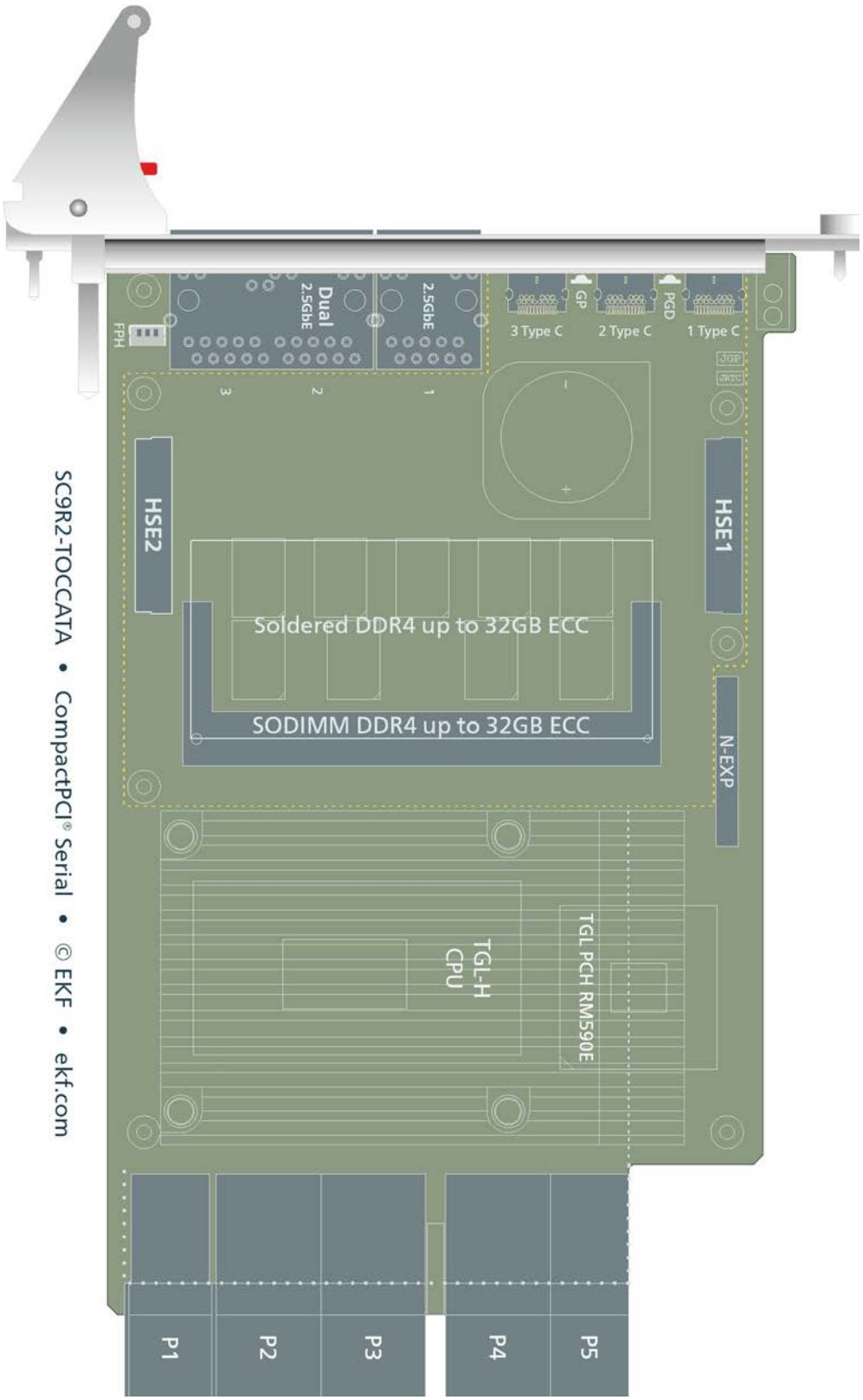


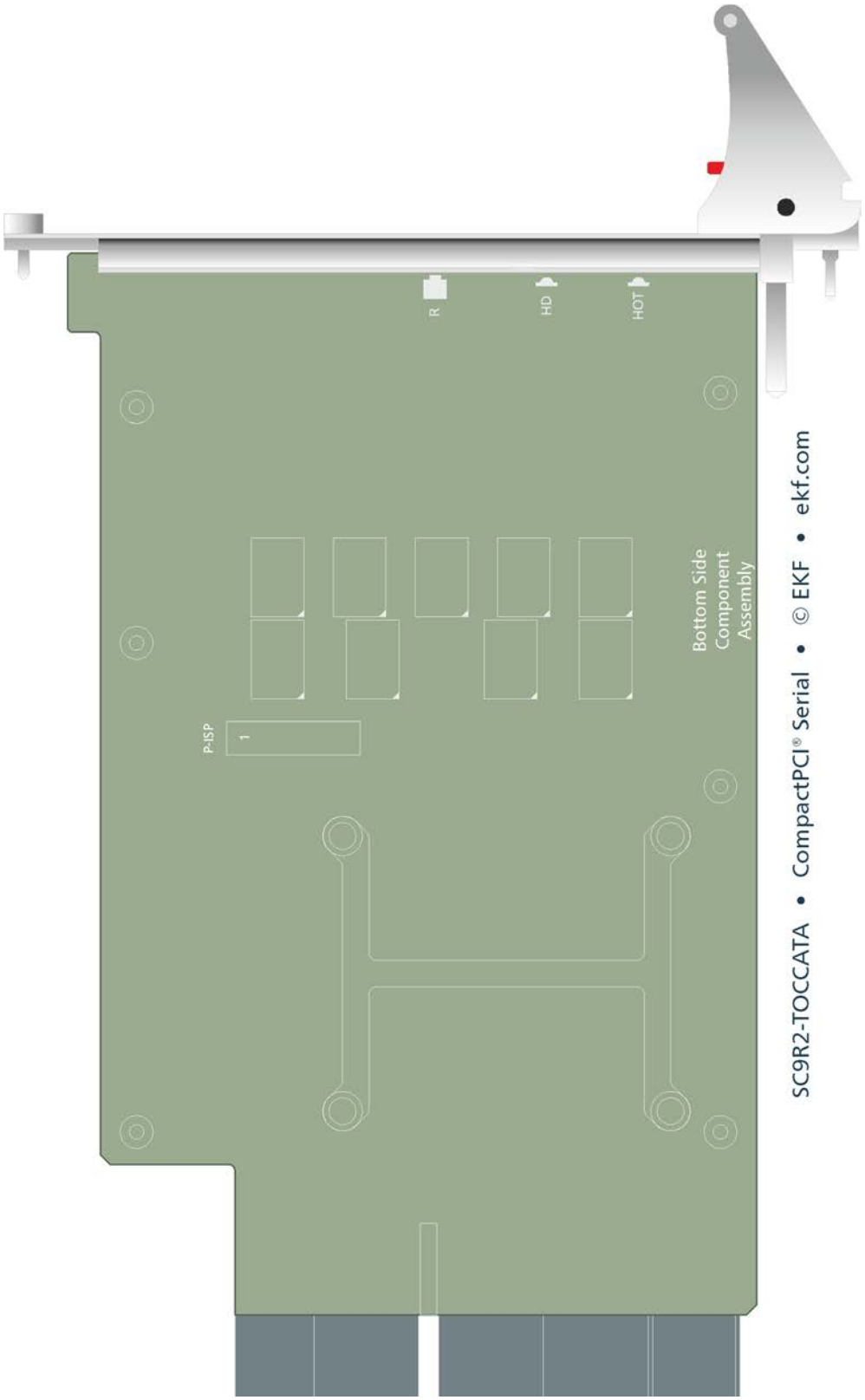
Front Panel Switches & Indicators

FPH	Front Panel Handle integrated microswitch (red button) Programmable function, power event button by default
GP	General Purpose bicolour LED
HD	LED indicating any activity on SATA ports
HT	LED indicating CPU or voltage regulator high temperature (yellow)
PG	Power Good/Board Healthy bicolour LED
RB	System Reset Button (Option)

LED			Status
PG Green/Red	GP Green/Red	HD Green	
OFF	GREEN	GREEN	Sleep State S5 (Soft Off)
OFF	GREEN	OFF	Sleep State S4 (Suspend to Disk/Hibernate)
OFF	OFF	GREEN	Sleep State S3 (Suspend to RAM/Standby)
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
YELLOW BLINK	X	X	Front panel handle is unlocked
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software Failure

Component Orientation

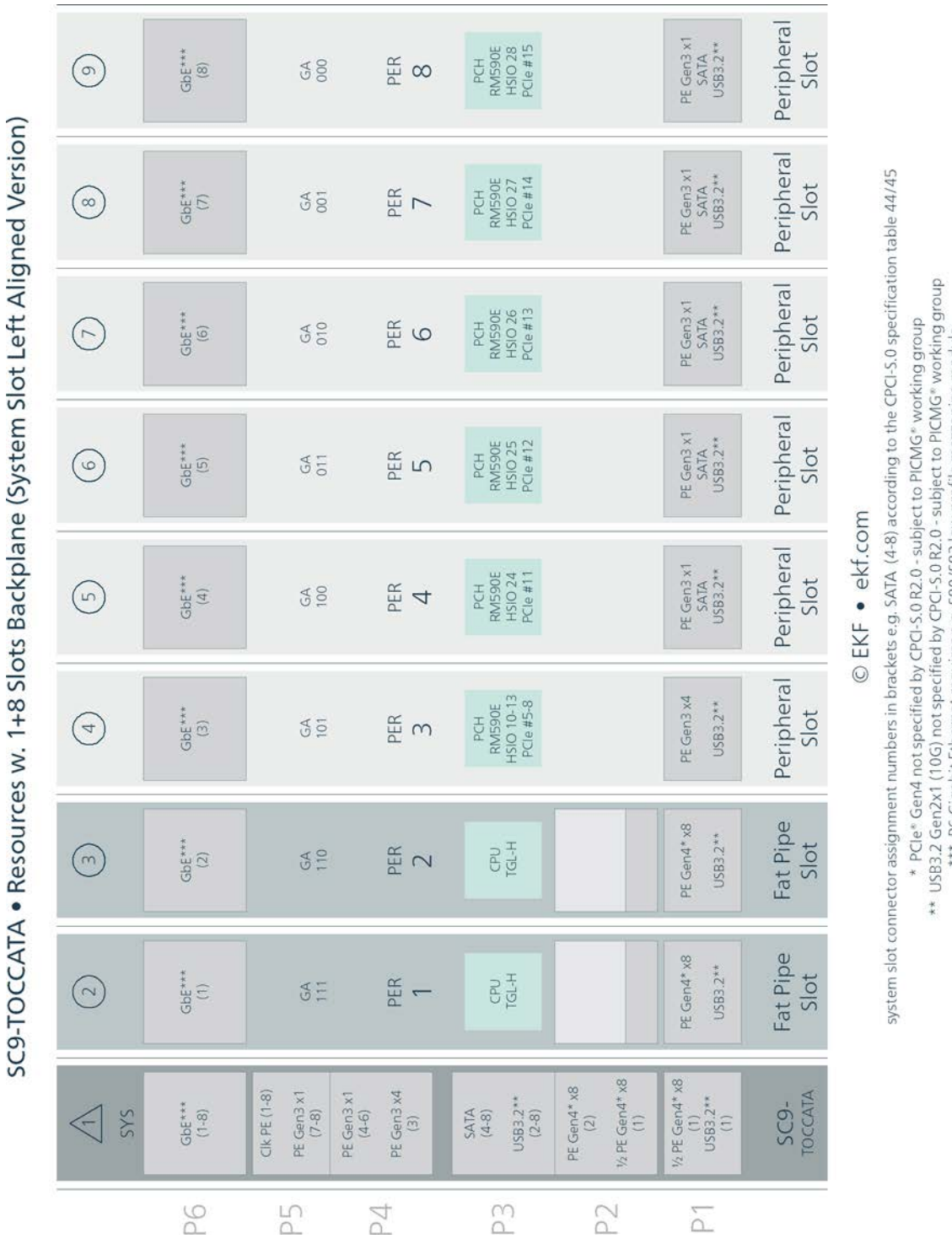



R
HD
HOT
P-ISP
1
Bottom Side
Component
Assembly
SC9R2-TOCCATA • CompactPCI® Serial • © EKF • ekf.com

Overview On-Board Connectors & Jumpers

N-EXP	Mezzanine	Utility Expansion Interface Connector (e.g. eSPI, HD Audio, SMBus) Interface to optional mezzanine side card
HSE1		High Speed Expansion Connector 1 (PCIe® Gen4 1x4, USB 3.2 Gen 2x1) Interface to low profile mezzanine module or side card
HSE2		High Speed Expansion Connector 2 (PCIe® Gen3 4x1, DisplayPort) Interface to optional low profile mezzanine module or side card
P1	Backplane	CompactPCI® Serial Type A Connector
P2-P4		CompactPCI® Serial Type B Connectors
P5		CompactPCI® Serial Type C Connector
P6		CompactPCI® Serial Type D Connector Option with a S8x-P6 series low profile mezzanine module
SODM	Memory	260-pin DDR4 ECC Memory Module (ECC SODIMM)
FPH	Handle	Connector to Front Panel Handle integrated switch
ISP	Manufacturing	In System Programming - bottom side manufacturing interface - not populated
J-MFG		Jumper to enter Manufacturing Mode, not populated
J-GP	Setup	Jumper to reset UEFI/BIOS setup to EKF factory defaults IEEE 1588 Pulse per Second Output
J-RTC		Jumper to reset RTC circuitry (part of PCH), not populated

Backplane Resources



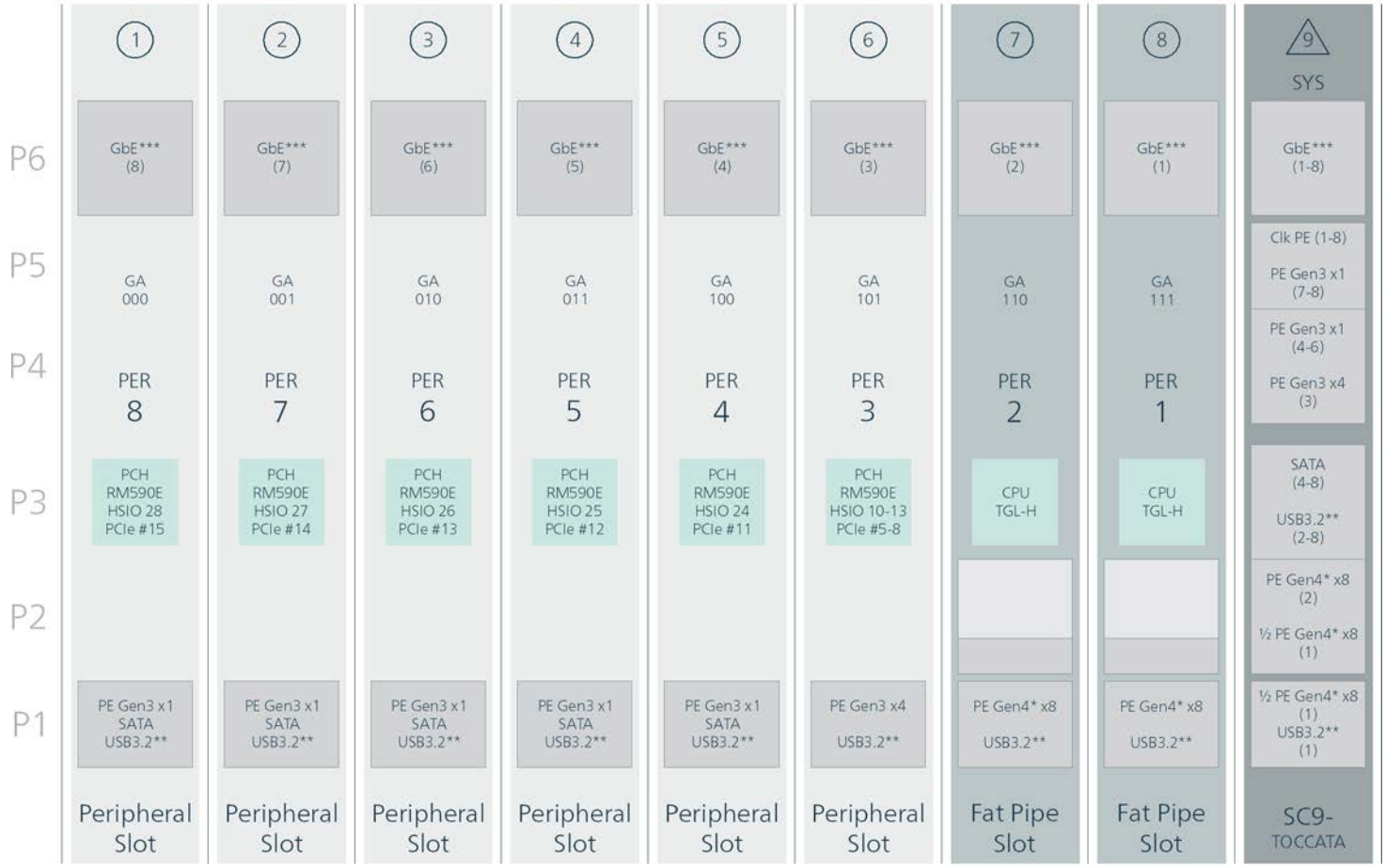
system slot connector assignment numbers in brackets e.g. SATA (4-8) according to the CPCI-5.0 specification table 44/45

* PCIe* Gen4 not specified by CPCI-5.0 R2.0 - subject to PICMG® working group

** USB3.2 Gen2x1 (10G) not specified by CPCI-5.0 R2.0 - subject to PICMG® working group

*** P6 Gigabit Ethernet requires e.g. S80/582 low profile mezzanine module

SC9-TOCCATA • Resources w. 1+8 Slots Backplane (System Slot Right Aligned Version)



system slot connector assignment numbers in brackets e.g. SATA (4-8) according to the CPCI-S.0 specification table 44/45

* PCIe® Gen4 not specified by CPCI-S.0 R2.0 - subject to PICMG® working group
** USB3.2 Gen2x1 (10G) not specified by CPCI-S.0 R2.0 - subject to PICMG® working group
*** P6 Gigabit Ethernet requires e.g. S80/S82 low profile mezzanine module

Microprocessor

The SC9-TOCCATA is equipped with an 11th generation Intel® mobile workstation XEON® W or Core™ processor (code name Tiger Lake H). These low power processors provide up to 8 cores running at turbo speeds up to 4.7GHz. The integrated graphics allow four 4k displays. 20 PCIe® Gen4 lanes are used for CompactPCI® Serial backplane support and SC9-TOCCATA local mezzanine expansion.

At the beginning, four processors are supported with different SC9-TOCCATA SKUs. The Tiger Lake H processors are housed in a BGA package for direct soldering to the PCB, i.e. the chip cannot be replaced by the user. On customers request, other processors are also available (refer to table 'Feature Summary', section 'Processor'.

Intel® XEON® W Processors (Industrial Use Case)										
EKF SKU	Processor	Cores	Clock GHz	Cache MB	Gfx MHz EU	Junction Temp. °C	TDP W	ECC	TCC/ TSN	vPro™
SC9-650D	W-11865MRE	8	4.7	24	1350 32	-40 to +100	45/35	✓	✓	✓
SC9-440D	W-11865MLE	8	4.5	24	1350 32	0 to +100	25	✓	✓	✓
SC9-340D	W-11555MLE	4	3.1	8	1250 16	0 to +100	25	✓	✓	✓

Intel® Core™ Processors (Embedded Use Case)										
EKF SKU	Processor	Cores	Clock GHz	Cache MB	Gfx MHz EU	Junction Temp. °C	TDP W	ECC	TCC/ TSN	vPro™
SC9-140D	6600HE	2	2.6	8	1100 16	0 to +100	35	-	-	-

Platform Controller Hub (PCH)

The SC9-TOCCATA is equipped with the RM590E Platform Controller Hub (Mobile Intel® 500 Series, industrial with Intel® vPro™). The PCH is attached to the Tiger Lake H processor via the DMI x8 Gen3.0 interface and provides up to 30 high speed I/O ports. 16 ports are used as PCIe® Gen3 lanes, on-board usage and backplane. Another 9 ports are in use for USB 3.2 10Gbps backplane and local mezzanine I/O. Five HSIO ports are dedicated to backplane SATA support.

The RM590E was chosen for extended temperature (T_j -40°C to +100°C) and Intel technologies support such as vPro™ (aka Intel® Active Management Technology) and TCC/TSN (Time Coordinated Computing / Time-Sensitive Networking).

Various internal devices are attached to the PCH e.g. SPI Flash memory (UEFI/BIOS/Firmware), or the Trusted Platform Module (TPM). Some legacy I/O such as UART, HD Audio, eSPI is wired from the PCH to the mezzanine expansion connector N-EXP.

Memory

The Tiger Lake H processors feature two channels x64 of DDR4 SDRAMs with support of ECC (Error Correction Code). On the SC9-TOCCATA, one channel is realized with up to 18 memory devices 8/16Gb soldered to the board (Memory Down) and delivers a capacity of up to 32GB at a clock frequency of 3200MHz.

The 2nd memory controller channel is wired to a socket, for installing an optional 260-pin ECC SODIMM module, thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR4 ECC SODIMMs (72-bit) with V_{DD}=1.2V featuring on-die termination (ODT), according the PC4-3200 specification. Maximum module size is 32GB. For best performance the module memory capacity should be equal/symmetric to the memory down capacity. Since the SODIMM socket may be hidden below a low profile mezzanine module or side card, it is recommended that the SODIMM module should be assembled by EKF.

By means of Intel® Total Memory Encryption (Intel® TME) all memory contents and instruction sets from CPU to memory are encrypted with AES 128-bit encryption. This is a hardware based method to protect against cold boot memory attacks.

In addition, the SC9-TOCCATA is equipped with SPI Flash non-volatile memory, for UEFI/BIOS and firmware storage.

Mass Storage

The SC9-TOCCATA base board is not provided with any mass storage device. Instead, EKF offers several low profile mezzanine modules such as the S48-SSD, with two M.2 sockets for PCIe® SSDs. Alternatively, peripheral boards are available for either SATA or PCIe® based mass storage, attached to CompactPCI® Serial backplane card slots.

Mezzanine mass storage comes as an assembly with the SC9-TOCCATA, either 4HP front panel width (low profile module), or 8HP (side card). Before ordering the SC9-TOCCATA, discuss your need for a low profile mezzanine mass storage module or side card with sales@ekf.com.

Graphics

The Tiger Lake H processors are provided with an Intel® X^e (Gen 12) graphics and media controller, for attachment of up to four DisplayPort™ 1.4a monitors. Three ports are available from the SC9-TOCCATA front panel, via Type-C receptacles (DP Alt Mode). For monitors w/o Type-C video connector use an adapter cable Type-C to DisplayPort™. Suitable Type-C cable connectors can be screw locked optionally via M2 threads in the front panel (single screw connector type for ports 1-3, dual screw type for port 4).

The 4th processor DisplayPort™ is wired to the SC9-TOCCATA mezzanine connector HSE2. By means of a low profile mezzanine module like the S40-NVME, a 4th DP Alt Mode Type-C receptacle would be available in the SC9-TOCCATA 4HP front panel.

The Tiger Lake H graphics controller supports up to

- 4 x 4k60 HDR
- 3 x 4k60 HDR
- 2 x 8k60 SDR /4k120 HDR /5k120 HDR
- 1 x 8k60 HDR

Graphics drivers can be downloaded from the Intel® website.

The front panel Type-C receptacles can be used for attachment of either DisplayPort™ monitors, or USB devices. Both signal groups are provided by the Tiger Lake H processor via multiplexers. With respect to USB, the SC9-TOCCATA front panel Type-C receptacles conform to USB 3.2 Gen 2x1 (10Gbps data transfer rate). Thunderbolt is not supported on the SC9-TOCCATA.

Networking

The SC9-TOCCATA is equipped with three I226-IT Networking Interface Controllers (NIC) wired to the front panel RJ45 jacks. Besides normal 4-speed networking (2.5GBASE-T, 1000BASE-T, 100BASE-TX, 10BASE-T) each Ethernet jack provides special features as listed below:

ETH 1	Wake on LAN (WoL), Intel® vPro™ capable (aka Intel® AMT)
ETH 2	TCC/TSN, this NIC is responsible also for PPS/PPM signal
ETH 3	TCC/TSN

TCC/TSN are both enhancements for low-latency operation, as required for real-time applications, e.g. OPC Unified Architecture and OpenAvnu.

TSN (Time-Sensitive Networking) refers to a collection of IEEE Ethernet standards:

802.1Qav	Credit-based Shaper for Bounded Latency
802.1 AS	Precision Time Protocol
802.1Qbv	Time-Aware Shaper
802.1Qbu/3br	Frame Preemption
802.3az	Energy-Efficient Ethernet

Intel® TCC (Intel® Time Coordinated Computing) defines additional in-system mechanisms for Time Synchronization and Timeliness.

If equipped with an S8x-P6 low profile mezzanine module, the SC9-TOCCATA in addition provides CompactPCI® Serial backplane Ethernet, either switch based, or via NICs. 8HP assembly mezzanine side cards such as the SCJ-VEENA allow to expand the number of front panel 2.5GbE jacks to seven in total.

Trusted Platform Module (TPM)

The SC9-TOCCATA provides a Trusted Platform Module according to TPM2.0. The Infineon Optiga™ SLx 9670 TPM2.0 is connected to the PCH by an SPI interface, and supports various cryptographic algorithms. The chip contains sophisticated cryptographic hardware modules (crypto processor and cryptographic engines) and is TPM2.0 compliant according to TCG test suites.

TPM Main Features

- Random Number Generator (RNG) according to NIST SP800-90A
- RSA-1024 and RSA-2048
- ECC NIST P256
- ECC BN256
- Compliant to TPM Main Specification, Family “2.0”, Level 00, Revision 1.38
- Certification according Common Criteria EAL4+

Serial ATA (SATA)

The SC9-TOCCATA provides five Serial ATA (SATA) ports for backplane usage, derived from the PCH. These ports support data transfer rates of 6Gbps (600MB/s), 3Gbps (300MB/s) or 1.5Gbps (150MB/s).

The HD status LED located in the front panel signals any disk activity of SATA devices attached as CompactPCI® Serial peripheral cards to the backplane.

PCI Express®

The SC9-TOCCATA is mainly based on PCI Express® (PCIe®) technology for on-board communication, CompactPCI® Serial backplane support, and mezzanine I/O expansion.

Twenty PCI Express® lanes are provided by the Tiger Lake H processor, organized as two links x8 for the two backplane fat pipe slots defined by CompactPCI® Serial. Another four lanes are wired to the expansion connector HSE1, as x4 link. All processor originated PCIe® lanes are Gen4 capable (16GT/s). With respect to the current CompactPCI® Serial specification R2.0, the backplane connectors are only Gen3 qualified however *. For low profile mezzanine expansion via HSE1, the Gen4 link can be utilised with a Gen4 M.2 SSD (e.g. S48-SSD low profile mezzanine module).

The RM590E PCH in addition offers several PCIe® Gen3 lanes (8GT/s) with flexible link width. These are wired to the on-board I226-IT Ethernet controllers, to the HSE2 high speed mezzanine expansion connector, and to the CompactPCI® Serial backplane connectors.

* The SC9-TOCCANA board design is ready for the coming CompactPCI® Serial specification R3.0, which complies with PCIe® Gen4/5 over the backplane. As VC1-TOCCATA this CPU card will be available with other backplane connectors, Gen4 capable.

Universal Serial Bus (USB)

The SC9-TOCCATA provides twelve USB 3 ports in total.

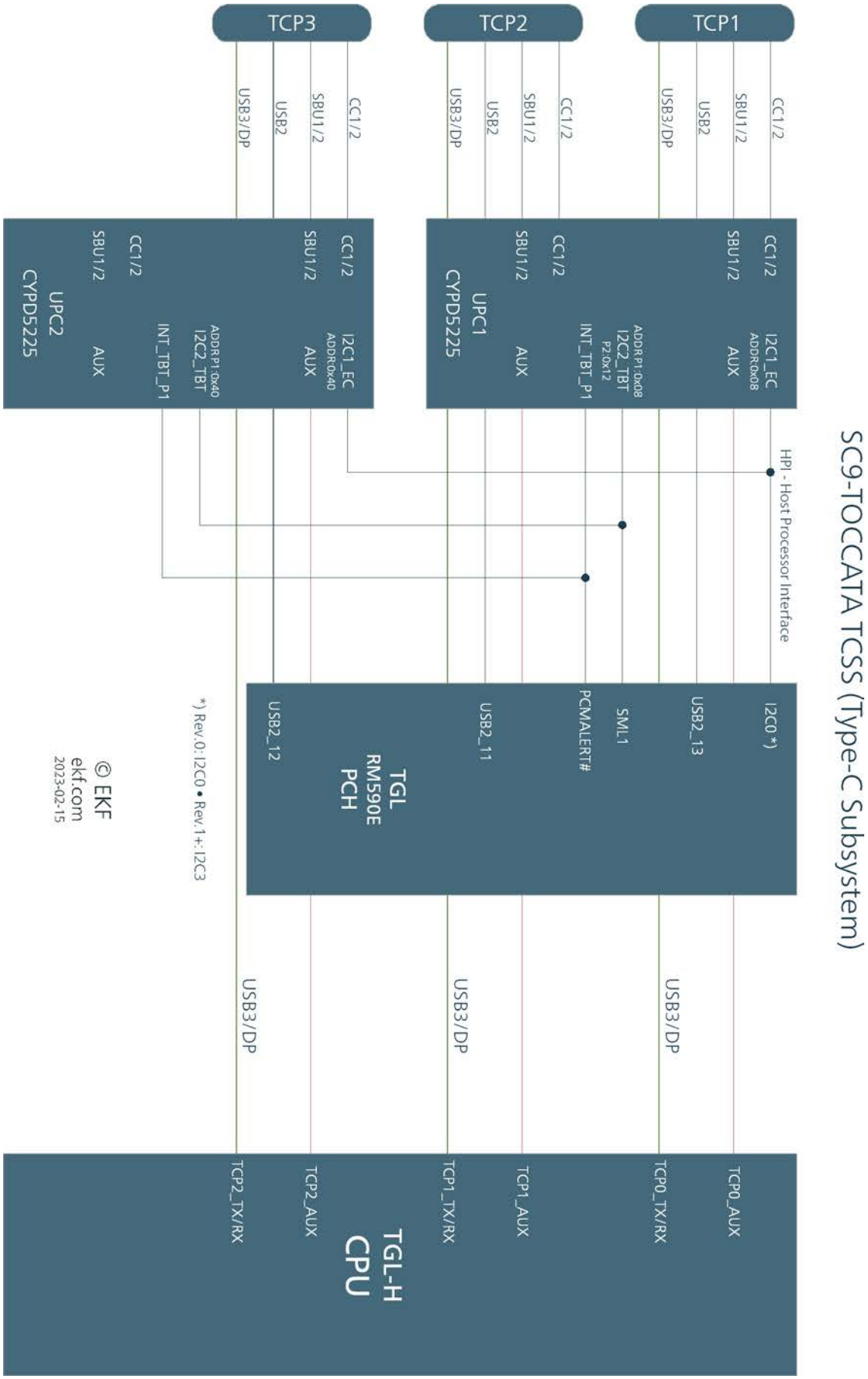
Three USB 3.2 Gen 2x1 (10Gbps data transfer rate) interfaces derived from the Tiger Lake H processor are wired to Type-C front panel connectors, multiplexed with video output signals (DP Alt Mode). These ports are assisted by power delivery controllers (USB-PD), configured for downstream facing applications. Each Infineon CYPD5225 (EZ-PD™ CCG5) has highly integrated subsystems according to the latest USB-PD standards. The maximum available V_{BUS} power for an attached device to any Type-C receptacle is 5V/3A (not concurrent an all ports). Adapters or adapter cables are throughout available for attachment of external devices with need for Type-A receptacles.

Another eight USB 3.2 Gen 2x1 (10Gbps data transfer rate) provided by the PCH are wired to the CompactPCI® Serial backplane connectors, hence USB3 is available on any peripheral slot.

Another USB 3.2 Gen 2x1 from the PCH is available via the HSE1 connector for mezzanine expansion.

Needless to say that each USB3 channel available with the SC9-TOCCATA is also USB2 capable.

TCSS (Type-C Subsystem)



SPI Flash

The SC9-TOCCATA is equipped with two non-volatile serial Flash memory devices, 128Mbit each, or (32MB in total, for UEFI/BIOS and firmware program storage. These components are attached to an PCH SPI port, and can be updated if necessary by the user. EKF provides programming tools and maintains BIOS long-term support with respect to feature updates and security issues.

https://www.ekf.com/s/sc9/firmware/

Real-Time Clock (RTC)

The SC9-TOCCATA has a time-of-day clock and 100-year calendar, integrated into the PCH. A battery on the board keeps the clock current when the computer is turned off. The SC9-TOCCATA uses a holder to keep a CR2032 lithium coin cell, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Alternately a CR2032 battery can be soldered to the board when board coating or shock/vibration is an interest.

In applications were the use of a battery is not permitted, a SuperCap can be soldered instead of the battery.

It is also possible to use the SC9-TOCCATA without any battery or SuperCap. In this case the Real-Time Clock can't keep its time and date. Per default an error message is reported by the UEFI/BIOS during boot in all cases, where the Real-Time clock settings are bad:

```
00C08270: Real Time Clock Error - Check Date and Time settings
00C08251: System CMOS Checksum bad
```

To suppress these messages a setup node exists within the UEFI/BIOS:

- After Power-On press function key <F2> to enter setup menu
- Advanced→Advanced Menu→Miscellaneous Options→Ignore Battery Error→Enabled
- Advanced→Advanced Menu→Management Engine Configuration→ME Unconfig on RTC Clear →Disabled

Replacement of the Battery

Some versions of SC9-TOCCATA are delivered with a battery holder for replacement of the coin cell. Use a CR2032 cell as replacement. Be careful when removing the old cell and inserting the new one. For boards with a soldered battery the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire. Battery cells could explode and cause personal injury!

Watchdog

An important reliability feature is a software programmable watchdog function. The SC9-TOCCATA contains two of these watchdogs. One is part of the PCH and also known as TCO watchdog. For a detailed description please refer to the 'Intel® 500 Series Chipset Family Platform Controller Hub' documentation. Operating systems e.g. Linux offer a driver interface to the TCO watchdog.

The behaviour of the 2nd watchdog is defined within a PLD of the SC9-TOCCATA, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After programming the time-out value and arming the WD, the related software (e.g. application program) must trigger the watchdog periodically. For details on programming the watchdog see section 'Technical Reference - Board Control and Status Register (BCSR)' in this manual.

This watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

Reset

To force a manual board reset, the SC9-TOCCATA offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The handle within the front panel contains a micro switch that is used to generate a power button event. By pressing the handles red push button a pulse is triggered.

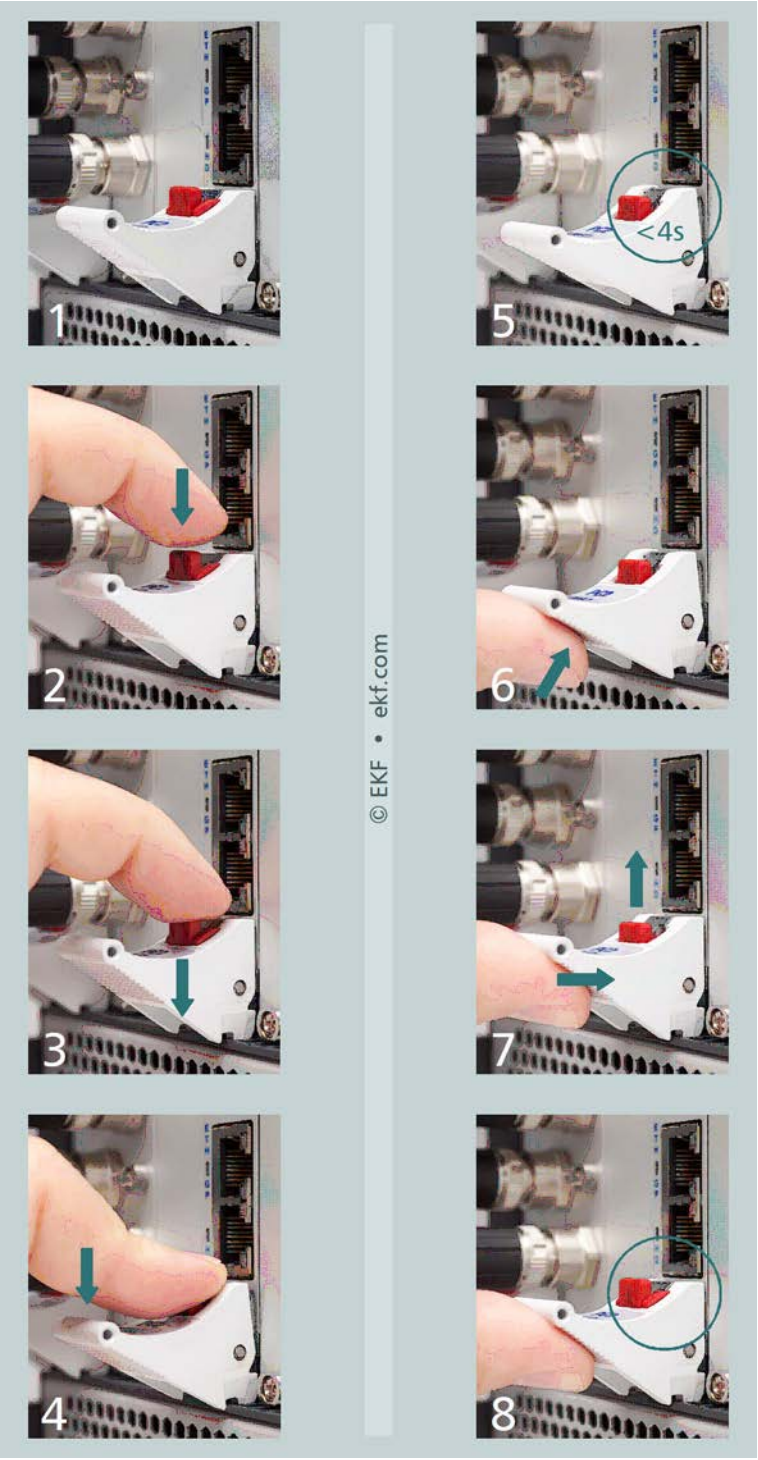
NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5 (Soft Off). In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the SC9-TOCCATA indicates the different power states.

The SC9-TOCCATA will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking ‘PG LED’.

The manual reset push-button and the power button functionality of the front panel handle could be reversed or passivated by UEFI/BIOS settings.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI® Serial connector P1 pin H2. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The SC9-TOCCATA is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.2V, 3.3V or 5V. The healthy state of the SC9-TOCCATA is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.



https://www.ekf.com/c/ccpu/img/reset_400.gif

Power Requirements

The SC9-TOCCATA must be supplied with +12V ±10% via its backplane connector P1. A maximum current value of 6.65A has been defined by the CompactPCI® Serial specification for a card slot. The maximum current actually required for the SC9-TOCCATA will be by far lower and depends on the particular processor populated and mezzanine expansion module in use.

For some applications a standby voltage +5V ±10% can be useful in addition, e.g. Wake-on-LAN. The maximum STANDBY current is defined as 0.95A by the CompactPCI® Serial specification. A standby power source is an option only and not mandatory for regular operation of the SC9-TOCCATA.

Main Power Supply Control (PS_ON#)

The SC9-TOCCATA draws its power from the +12V main supply rail defined by the CompactPCI® Serial specification. The board has been designed to control this main power supply by use of the signal PS_ON# (backplane connector P1 pin E2). If the system enters the sleep state S5 (Soft Off), the signal PS_ON# is pulled high, hence the main power supply is switched-off. The SC9-TOCCATA is held in soft off state until a power management event (e.g. power button event triggered by the front panel handle) brings back the system to the S0 state.

In order to work as described above and to generate clean signals on PS_ON#, the +5V standby voltage (STANDBY) mentioned above is necessary. This optional power rail, tied to connector P1 pin B1, is also part of the CompactPCI® Serial specification. The stand-by power rail must be always switched-on, independent of the state of PS_ON#.

Nevertheless, STANDBY is not mandatory to operate the SC9-TOCCATA. If no standby power is available, the board creates this voltage from the main power rail. In this case it is important that the PS_ON# signal is pulled down somewhere in the system or the power supply delivers its voltage independent of a PS_ON# signal.

Power Supply Status (PWR_FAIL#)

Power supply failures may be detected before the system crashes down by monitoring the signal PWR_FAIL#. This active low line (connector P1 pin F3) is an addition to the CompactPCI® Serial specification and may be driven by the power supply. PWR_FAIL# signals the possible failure of the main supply voltage +12V. On the SC9-TOCCATA the signal PWR_FAIL# is routed to GPP_D7 of the PCH to analyse the state of the power supply unit.

Thermal Considerations

In order to avoid malfunctioning of the SC9-TOCCATA, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers or via PECI bus. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors, one of it located in the system hardware monitor NCT7491, allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the NCT7491 also keeps a PECI 3.0 master for CPU DTS monitoring and supervises most of the supply voltages. A suitable tool on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, would be HWiNFO64, which can be downloaded from the web.

The SC9-TOCCATA is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CompactPCI® Serial board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>20m^3/h or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

For high performance applications also 8HP heatsink solutions are available.

Peripheral Slot Operation

Beyond the typical role as system slot card, the SC9-TOCCATA is operable in periphery slots as well. In this case it acts as a satellite system, linked to other (processor-) boards by its backplane Ethernet connections. The other resources associated with the backplane like PCI Express®, SATA or USB are not usable in this situation.

Some of the following, system slot dedicated control signals get an altered function or will be disconnected from the backplane:

- PWRBTN# (Connector P1 Pin C3) becomes GA0
- PWR_FAIL# (Connector P1 Pin F3) becomes GA1
- PRST# (Connector P1 Pin H2) becomes RST# and will be disconnected
- WAKE# (Connector P1 Pin I2) will be disconnected

One result of that is, that a SC9-TOCCATA plugged into a peripheral slot will not get a reset even if the system controller forces the reset signal on the backplane to an active state.

Board Hot-Plug

Hot-plug of the SC9-TOCCATA itself is not supported, no matter whether it is working as a system controller or satellite board. But the SC9-TOCCATA can detect and handle hot-plug events of CompactPCI® Serial peripheral cards. This feature is supported on all interfaces fed to the backplane, i.e.

- PCI Express®
- SATA
- USB 2/3
- Gigabit Ethernet

Apart from PCI Express®, hot-plug is enabled on the other interfaces by default. For PCIe® the UEFI/BIOS setup of the SC9-TOCCATA provides settings to switch on or off the hot-plug feature, for Fat Pipe or Standard peripheral slots on different menu places:

- After Power-On press function key <F2> to enter setup menu
- Fat Pipe Slots:
  Advanced→Advanced Menu→PCI Configuration→SA PCI Express Configuration→Hot-Plug
- Standard Slots:
  Advanced→Advanced Menu→PCI Configuration→PCH PCI Express Configuration
  PCH PCIe Root Port [5-8/11-15]→Hot-Plug

Supplementary Information

Related Information	
SC9-TOCCATA Home	https://www.ekf.com/s/sc9/sc9.html
S20-NVME Low Profile Mezzanine	https://www.ekf.com/s/s20/s20.html
S40-NVME Low Profile Mezzanine	https://www.ekf.com/s/s40/s40.html
S42-MC Low Profile Mezzanine	https://www.ekf.com/s/s42/s42.html
S48-SSD Low Profile Mezzanine	https://www.ekf.com/s/s48/s48.html
S80-P6 Low Profile Mezzanine	https://www.ekf.com/s/s80/s80.html
S82-P6 Low Profile Mezzanine	https://www.ekf.com/s/s82/s82.html
S83-P6 Low Profile Mezzanine	https://www.ekf.com/s/s83/s83.html
S84-P6 Low Profile Mezzanine	*1 x 10G Backplane Ethernet (KR)*
S85-P6 Low Profile Mezzanine	*4 x 5G Backplane Ethernet (5GBASE-T)*
SCG-MULTIGIG Mezzanine Side Card	*2 x 10GBASE-T M12-X*
SCI-MULTIGIG Mezzanine Side Card	*2 x 10GBASE-T RJ45*
SCJ-VEENA Mezzanine Side Card	https://www.ekf.com/s/scj/scj.html
SCL-RHYTHM Mezzanine Side Card	https://www.ekf.com/s/scl/scl.html
SCX-PCIE Mezzanine Side Card	https://www.ekf.com/s/scx/scx.html
SCZ-NVM Mezzanine Side Card	https://www.ekf.com/s/scz/scz.html
ECX-PCIE Mezzanine Side Card	https://www.ekf.com/e/ecx/ecx.html
Mezzanine Connectors Explained	https://www.ekf.com/s/mezzanine_connectors.pdf

General Information CompactPCI® Serial	
CompactPCI® Serial Concise Overview	https://www.ekf.com/s/serial_concise.pdf
CompactPCI® Serial All You Need to Know	https://www.ekf.com/s/smart_solution.pdf
CompactPCI® Serial Home	https://www.ekf.com/s/serial.html

Ordering Information
For popular SC9-TOCCATA SKUs please refer to https://www.ekf.com/liste/liste_21.html#SC9
For new mezzanine connector based low profile modules please refer to https://www.ekf.com/liste/liste_21.html#S20

Technical Reference

Local PCI® Devices

The following table shows the on-board PCI® devices and their location within the PCI® configuration space. Several devices are part of the processor and platform controller hub RM590E (Mobile Series 500 PCH).

Bus	Device	Function	Vendor	Device	Description
0	0	0	0x8086	0x9A36	Processor Host Bridge/DRAM Controller
0	1	0	0x8086	0x9A01	Processor PCI Express Controller (→ x8 CPCI-S.0)
0	1	1	0x8086	0x9A05	Processor PCI Express Controller (→ x8 CPCI-S.0)
0	2	0	0x8086	0x9A60	Processor Integrated Graphics Device
0	6	0	0x8086	0x9A0F	Processor PCI Express Controller (→ x4 HSE1)
0	8	0	0x8086	0x9A11	Gaussian Mixture Model Device
0	13	0	0x8086	0x9A17	USB 3.2 xHCI Gen 2 Controller (→ Type-C Sub System)
0	20	0	0x8086	0x43ED	USB 3.2 xHCI Gen 2 Controller
0	20	2	0x8086	0xA131	Thermal Subsystem
0	21	0-1	0x8086	0x43E8-43E9	I^2C Controller #0-1
0	22	0-1	0x8086	0x43E0-43E1	Intel CSME Interface #1-2
0	22	2	0x8086	0x43E2	Intel CSME IDE Redirection
0	22	3	0x8086	0x43E3	Intel CSME Keyboard Text Redirection
0	22	4-5	0x8086	0x43E4-43E5	Intel CSME Interface #3-4
0	23	0	0x8086	0x43D3 0x43D7	SATA: AHCI Mode [1] SATA: RAID 0/1/5/10 Capable [2]
0	27	0-3	0x8086	0x43C4-43C7	PCH PCI Express Root Port #21-24 (→ x4 HSE2)
0	28	0	0x8086	0x43BB	PCH PCI Express Port #4 (→ Intel i226IT)
0	28	4-7	0x8086	0x43BC-43BF	PCH PCI Express Port #5-8 (→ x4 CPCI-S.0)
0	29	0-1	0x8086	0x43B0-43B1	PCH PCI Express Port #9-10 (→ 2x Intel i226IT)
0	29	2-6	0x8086	0x43B2-43B6	PCH PCI Express Port #11-15 (→ x1 CPCI-S.0)
0	30	0-1	0x8086	0x43A8-43A9	UART Controller #0-1
0	31	0	0x8086	0x438x	eSPI Controller
0	31	3	0x8086	0x43C8	Intel High Definition Audio
0	31	4	0x8086	0x43A3	SMBus Controller
0	31	5	0x8086	0x43A3	SPI (Flash) Controller
2 [3]	00	0	0x8086	0x125D	Ethernet Controller NC1 (Intel i226IT)
3 [3]	00	0	0x8086	0x125D	Ethernet Controller NC2 (Intel i226IT)
4 [3]	00	0	0x8086	0x125D	Ethernet Controller NC3 (Intel i226IT)

1) Depends on UEFI/BIOS settings.

2) Depending on UEFI/BIOS settings different RAID modes may lead to other Device IDs.

3) Bus number can vary depending on the PCI enumeration schema implemented in UEFI/BIOS.

Local SMB/I²C Devices

The SC9-TOCCATA contains devices that are attached to the System Management Bus (SMBus). These are the SPD EEPROMs for the on-board memory or the possibly plugged SODIMM, a general purpose serial EEPROM containing board configuration data, the supply voltage/temperature monitoring device NCT7491, a counter for operating hours and reset events, a set of board control and status registers as well as two dual general purpose, non-volatile electronic jumpers. Additional devices may be connected to the different I²C controllers of the RM590E via the CompactPCI® Serial backplane signals I²C_SCL (P1 B2) and I²C_SDA (P1 C2) or the mezzanine expansion connectors HSE2 or N-EXP.

Controller	Address	Description
SMBus	0x23	Non-volatile Electronic Jumpers 3/4
SMBus	0x2C	Hardware Monitor/Memory Down Temperature Sensor (NCT7491)
SMBus	0x2E	Board Control/Status
SMBus	0x2F	Non-volatile Electronic Jumpers 1/2
SMBus	0x50 0x30	SPD EEPROM of On-board Memory 4KBit EEPROM Select Bank 0/1
SMBus	0x52 0x32	SPD EEPROM of SODIMM 4KBit EEPROM Select Bank 0/1
SMBus	0x57	General Purpose EEPROM 2KBit
SMBus	0x6B	operating hours/reset counters (DS1683)
I2C[0]	[1)]	P-HSE2 (Pins A22/A23), N-EXP (Pins 29/30)
I2C[1]	[1)]	Serial Backplane Connector P1 (Pins B2/C2)

[1)] Address depends on devices attached

Hardware Monitor NCT7491

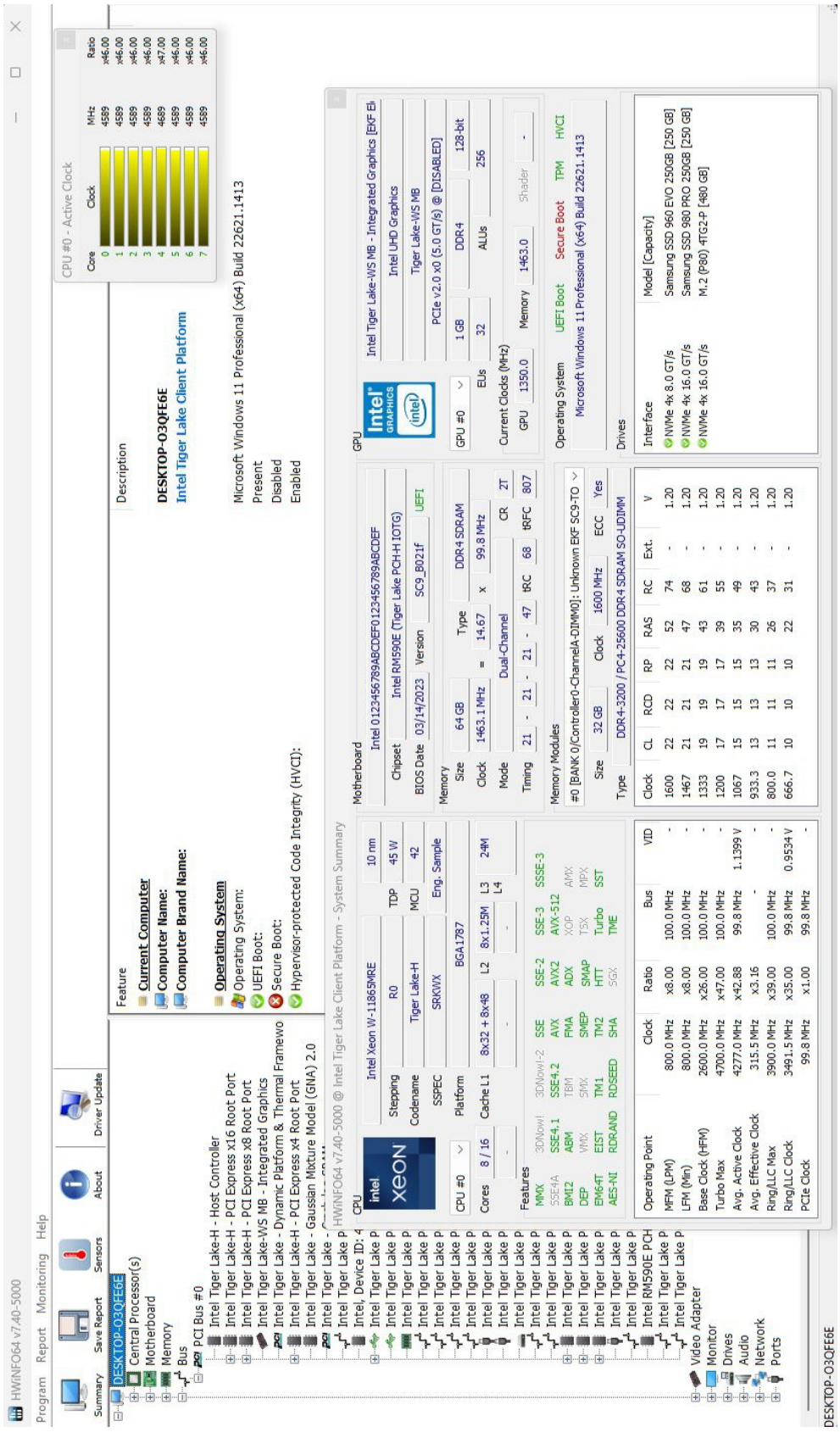
Attached to the SMBus, the SC9-TOCCATA is provided with the hardware monitor NCT7491. This device is capable to observe the temperatures of the board, processor cores, and on-board memory, as well as several supply voltage rails with a resolution of 10 bit. The following table shows the mapping of the voltage inputs of the NCT7491 to the corresponding supply voltages of the SC9-TOCCATA:

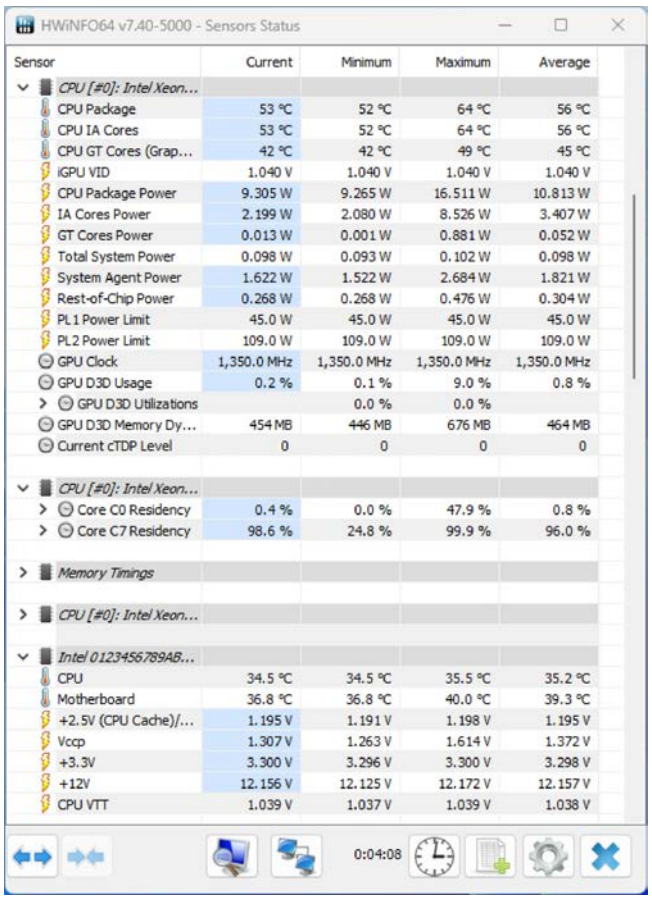
Input	Source	Resolution	Register (MSB/LSB)
VCCP	Processor Core Voltage	2.93mV	0x21/0x76[3:2]
VTT	Processor Sustain Voltage (+1.05V)	2.20mV	0x1E/0x1F[5:4]
+2.5V/THERM#	+1.2V	3.26mV	0x20/0x76[1:0]
VCC	+3.3V	4.29mV	0x22/0x76[5:4]
+5Vin	Coin Cell Voltage (V_{CCRTC})	6.54mV	0x23/0x76[7:6]
+12Vin	+12V	15.92mV	0x24/0x77[1:0]
PECI	Core #0 absolute Temperature	1°C	0x04
PECI	Core #1 absolute Temperature	1°C	0x05
PECI	Core #2 absolute Temperature	1°C	0x06
PECI	Core #3 absolute Temperature	1°C	0x07
D1+/D1-	Memory Down absolute Temperature	0.25°C	0x25/0x77[3:2]
Local TEMP	SC9 Surface Temperature	0.25°C	0x26/0x77[5:4]

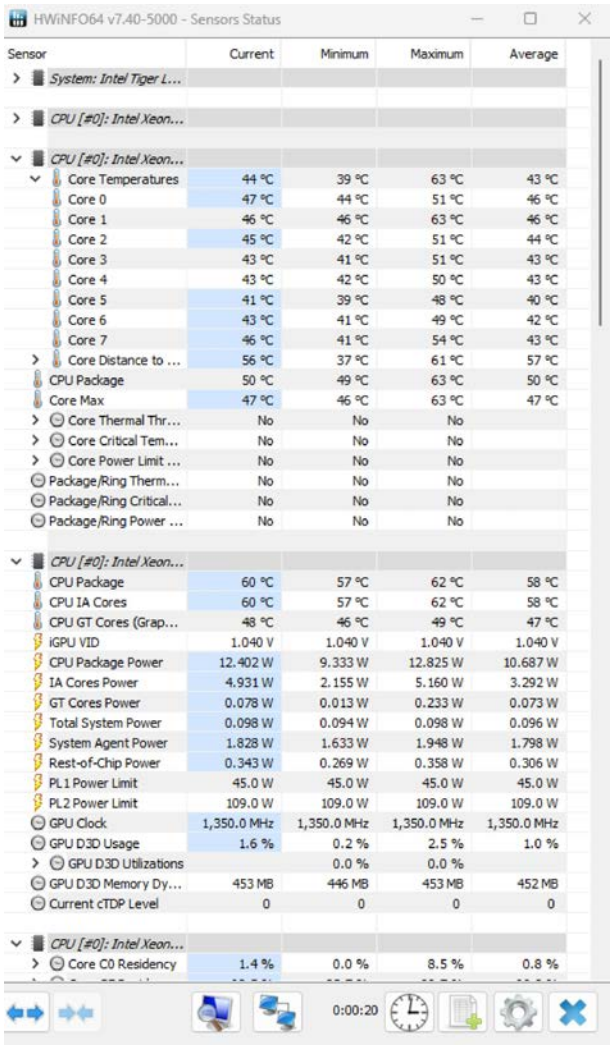
Besides continuous measuring of temperatures and voltages the NCT7491 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the NCT7491 can request an over-temperature event on GPP_D11 input of the RM590E PCH or an interrupt via the GPP_D12 input (which may result in a system management interrupt).

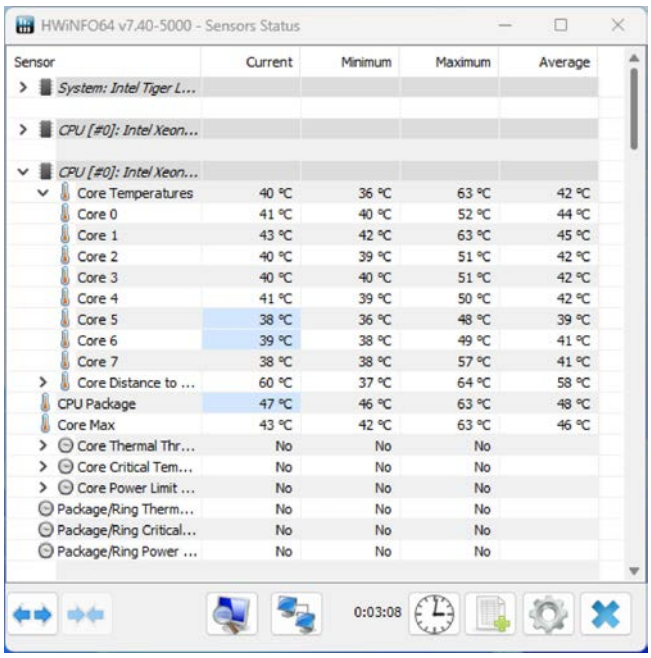
Hardware Diagnostics Tool HWiNFO

Available as 3rd party professional system information and diagnostics tool for the SC9-TOCCATA, EKF recommends HWiNFO (https://www.hwinfo.com/). For commercial use, the program must be licenced (https://www.hwinfo.com/licenses/). Sample HWiNFO screenshots captured from a SC9-TOCCATA running Windows11 are provided below:




HWiNFO64 v7.40-5000 - Sensors Status
Sensor | Current | Minimum | Maximum | Average
CPU [#0]: Intel Xeon...
CPU Package | 53 °C | 52 °C | 64 °C | 56 °C
CPU IA Cores | 53 °C | 52 °C | 64 °C | 56 °C
CPU GT Cores (Grap... | 42 °C | 42 °C | 49 °C | 45 °C
iGPU VID | 1.040 V | 1.040 V | 1.040 V | 1.040 V
CPU Package Power | 9.305 W | 9.265 W | 16.511 W | 10.813 W
IA Cores Power | 2.199 W | 2.080 W | 8.526 W | 3.407 W
GT Cores Power | 0.013 W | 0.001 W | 0.881 W | 0.052 W
Total System Power | 0.098 W | 0.093 W | 0.102 W | 0.098 W
System Agent Power | 1.622 W | 1.522 W | 2.684 W | 1.821 W
Rest-of-Chip Power | 0.268 W | 0.268 W | 0.476 W | 0.304 W
PL1 Power Limit | 45.0 W | 45.0 W | 45.0 W | 45.0 W
PL2 Power Limit | 109.0 W | 109.0 W | 109.0 W | 109.0 W
GPU Clock | 1,350.0 MHz | 1,350.0 MHz | 1,350.0 MHz | 1,350.0 MHz
GPU D3D Usage | 0.2 % | 0.1 % | 9.0 % | 0.8 %
GPU D3D Utilizations | | 0.0 % | 0.0 % |
GPU D3D Memory Dy... | 454 MB | 446 MB | 676 MB | 464 MB
Current cTDP Level | 0 | 0 | 0 | 0
CPU [#0]: Intel Xeon...
Core C0 Residency | 0.4 % | 0.0 % | 47.9 % | 0.8 %
Core C7 Residency | 98.6 % | 24.8 % | 99.9 % | 96.0 %
Memory Timings
CPU [#0]: Intel Xeon...
Intel 0123456789AB...
CPU | 34.5 °C | 34.5 °C | 35.5 °C | 35.2 °C
Motherboard | 36.8 °C | 36.8 °C | 40.0 °C | 39.3 °C
+2.5V (CPU Cache)/... | 1.195 V | 1.191 V | 1.198 V | 1.195 V
Vccp | 1.307 V | 1.263 V | 1.614 V | 1.372 V
+3.3V | 3.300 V | 3.296 V | 3.300 V | 3.298 V
+12V | 12.156 V | 12.125 V | 12.172 V | 12.157 V
CPU VTT | 1.039 V | 1.037 V | 1.039 V | 1.038 V
0:04:08


HWiNFO64 v7.40-5000 - Sensors Status
Sensor | Current | Minimum | Maximum | Average
System: Intel Tiger L...
CPU [#0]: Intel Xeon...
CPU [#0]: Intel Xeon...
Core Temperatures | 44 °C | 39 °C | 63 °C | 43 °C
Core 0 | 47 °C | 44 °C | 51 °C | 46 °C
Core 1 | 46 °C | 46 °C | 63 °C | 46 °C
Core 2 | 45 °C | 42 °C | 51 °C | 44 °C
Core 3 | 43 °C | 41 °C | 51 °C | 43 °C
Core 4 | 43 °C | 42 °C | 50 °C | 43 °C
Core 5 | 41 °C | 39 °C | 48 °C | 40 °C
Core 6 | 43 °C | 41 °C | 49 °C | 42 °C
Core 7 | 46 °C | 41 °C | 54 °C | 43 °C
Core Distance to ... | 56 °C | 37 °C | 61 °C | 57 °C
CPU Package | 50 °C | 49 °C | 63 °C | 50 °C
Core Max | 47 °C | 46 °C | 63 °C | 47 °C
Core Thermal Thr... | No | No | No
Core Critical Tem... | No | No | No
Core Power Limit ... | No | No | No
Package/Ring Therm... | No | No | No
Package/Ring Critical... | No | No | No
Package/Ring Power ... | No | No | No
CPU [#0]: Intel Xeon...
CPU Package | 60 °C | 57 °C | 62 °C | 58 °C
CPU IA Cores | 60 °C | 57 °C | 62 °C | 58 °C
CPU GT Cores (Grap... | 48 °C | 46 °C | 49 °C | 47 °C
iGPU VID | 1.040 V | 1.040 V | 1.040 V | 1.040 V
CPU Package Power | 12.402 W | 9.333 W | 12.825 W | 10.687 W
IA Cores Power | 4.931 W | 2.155 W | 5.160 W | 3.292 W
GT Cores Power | 0.078 W | 0.013 W | 0.233 W | 0.073 W
Total System Power | 0.098 W | 0.094 W | 0.098 W | 0.096 W
System Agent Power | 1.828 W | 1.633 W | 1.948 W | 1.798 W
Rest-of-Chip Power | 0.343 W | 0.269 W | 0.358 W | 0.306 W
PL1 Power Limit | 45.0 W | 45.0 W | 45.0 W | 45.0 W
PL2 Power Limit | 109.0 W | 109.0 W | 109.0 W | 109.0 W
GPU Clock | 1,350.0 MHz | 1,350.0 MHz | 1,350.0 MHz | 1,350.0 MHz
GPU D3D Usage | 1.6 % | 0.2 % | 2.5 % | 1.0 %
GPU D3D Utilizations | | 0.0 % | 0.0 % |
GPU D3D Memory Dy... | 453 MB | 446 MB | 453 MB | 452 MB
Current cTDP Level | 0 | 0 | 0 | 0
CPU [#0]: Intel Xeon...
Core C0 Residency | 1.4 % | 0.0 % | 8.5 % | 0.8 %
0:00:20


HWiNFO64 v7.40-5000 - Sensors Status
Sensor | Current | Minimum | Maximum | Average
System: Intel Tiger L...
CPU [#0]: Intel Xeon...
CPU [#0]: Intel Xeon...
Core Temperatures | 40 °C | 36 °C | 63 °C | 42 °C
Core 0 | 41 °C | 40 °C | 52 °C | 44 °C
Core 1 | 43 °C | 42 °C | 63 °C | 45 °C
Core 2 | 40 °C | 39 °C | 51 °C | 42 °C
Core 3 | 40 °C | 40 °C | 51 °C | 42 °C
Core 4 | 41 °C | 39 °C | 50 °C | 42 °C
Core 5 | 38 °C | 36 °C | 48 °C | 39 °C
Core 6 | 39 °C | 38 °C | 49 °C | 41 °C
Core 7 | 38 °C | 38 °C | 57 °C | 41 °C
Core Distance to ... | 60 °C | 37 °C | 64 °C | 58 °C
CPU Package | 47 °C | 46 °C | 63 °C | 48 °C
Core Max | 43 °C | 42 °C | 63 °C | 46 °C
Core Thermal Thr... | No | No | No
Core Critical Tem... | No | No | No
Core Power Limit ... | No | No | No
Package/Ring Therm... | No | No | No
Package/Ring Critical... | No | No | No
Package/Ring Power ... | No | No | No
0:03:08

Board Control and Status Registers (BCSR)

A set of board control and status registers allow to program special features on the SC9-TOCCATA:

- Assert a full reset
- Control activity of front panel reset and power event button
- Program time-outs and trigger a watchdog
- Get access to two LEDs in the front panel
- Get power fail and watchdog status of last board reset

The register set consists of five registers located on the SMBus at Device ID=0x2E on the following addresses:

- 0xA0: CMD_CTRL0_WR: Write to Control Register 0 (Write-Only)
- 0xA1: CMD_CTRL0_RD: Read from Control Register 0 (Read-Only)
- 0xB0: CMD_STAT0_WR: Write to Status Register 0 (Write-Clear)
- 0xB1: CMD_STAT0_RD: Read from Status Register 0 (Read-Only)
- 0xB2: CMD_STAT1_WR: Write to Status Register 1 (Write-Clear)
- 0xB3: CMD_STAT1_RD: Read from Status Register 1 (Read-Only)
- 0xC1: CMD_PLDREV_RD: Read from PLD Revision Register (Read-Only)

To prevent malfunction, access to these registers should be done by SMBus “Byte Data” commands. Further more, writes to read-only or reads to write-only registers should be avoided.

Write/Read Control Register 0

Write: SMBus Address 0xA0 Default after reset: 0x00

Read: SMBus Address 0xA1

Bit	Description CMD_CTRL0
7	GPLED 0=Green part of the front panel LED GP is off (Default) 1=Green part of the front panel LED GP is on
6	FPDIS 0=Enable the front panel handle switch (Default) 1=Disable the front panel handle switch
5	FERP# 0=The front panel handle switch generates a power event (Default) 1=The front panel handle switch generates a system reset
4:3	WDGT0:WDGT1 Maximum Watchdog retrigger time: 0:0 2 sec 1:0 10 sec 0:1 50 sec 1:1 250 sec
2	WDGTRG Retrigger Watchdog. Any change of this bit will retrigger the watchdog. After a system reset the watchdog is in an inactive state. The watchdog is armed on the 1st edge of this bit.
1	PGLED 0=Red part of the front panel LED PG is off (Default) 1=Red part of the front panel LED PG is blinking
0	SRES 0=Normal operation (Default) 1=A full system reset is performed

Read/Clear Status Register 0

Write: SMBus Address 0xB0

Read: SMBus Address 0xB1

Bit	Description CMD_STAT0
7	RESERVED Always read as 0
6	RESERVED Always read as 0
5	PF18A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.8A voltage regulator
4	PF25S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V2.5S4 voltage regulator
3	PF12S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.2S4 voltage regulator
2	PFVRST 0=Normal operation 1=Last system reset may be caused by a power failure of the +VCCST_CPU load switch
1	PFVRAX 0=Normal operation 1=Last system reset may be caused by a power failure of the IMVP-9 +VCCAUX voltage regulator
0	PFVRC 0=Normal operation 1=Last system reset may be caused by a power failure of the IMVP-9 +VCC_CPU voltage regulator

The bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read/Clear Status Register 1

Write: SMBus Address 0xB2
Read: SMBus Address 0xB3

Bit	Description CMD_STAT1
7	WDGARMD 0=Normal operation 1=The watchdog is armed and has to be retriggered within its time-out period
6	WDGRST 0=Normal operation 1=Last system reset may be caused by a watchdog time-out
5	WDGHT 0=Normal operation 1=The watchdog already has elapsed half of its time-out period
4	PF5PS 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5PS voltage regulator
3	PF5S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5S voltage regulator
2	PF33A1 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3A1ST voltage regulator
1	PF33A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3A load switch
0	PF33S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3S voltage regulator

Except of WDGHT and WDGARMD the bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read PLD Revision Register

Write: Not allowed

Read: SMBus Address 0xC1

Bit	Description CMD_PLDREV
7:0	PLDREV Read PLD Revison Number

Configuration Jumpers

J-GP - Loading UEFI/BIOS Setup Defaults & IEEE 1588 Pulse per Second

The jumper J-GP may be used to reset the UEFI/BIOS configuration settings to a default state. The UEFI/BIOS on SC9-TOCCATA stores most of its settings in an area within the UEFI/BIOS flash, e.g. the actual boot devices. Using the jumper J-GP is only necessary, if it is not possible to enter the setup of the UEFI/BIOS. To reset the settings mount a jumper on J-GP and perform a system reset. As long as the jumper is stuffed the UEFI/BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.

To fulfill the above functionality pin 1 of J-GP (the pin with the square pad) is connected to GPP_D18 of the RM590E.

There is also an alternate function available on J-GP. Pin 1 of this jumper carries a Pulse per Second (PPS) signal according the IEEE 1588 specification when enabled by UEFI/BIOS settings. A wire may be connected to trigger events on external devices.

NOTE: The PPS signal is also available at the CompactPCI® Serial connector P1 pin J3 (SATA-SCL).

J-GP	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	UEFI/BIOS configuration reset performed

[1)] This setting is the factory default

J-MFG - Manufacturer Mode Jumper

The jumper J-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed. The pin header J-MFG is not stuffed on the SC9-TOCCATA by default.

J-MFG	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	Entering Manufacturer Mode

[1)] This setting is the factory default

J-RTC - RTC Reset

The jumper J-RTC may be used to reset certain register bits of the battery backed RTC core within the PCH RM590E. This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the UEFI/BIOS POST after power on. Note that installing of jumper J-RTC will neither set UEFI/BIOS Setup to EKF Factory Defaults nor resets the time and date register values of the RTC (Real Time Clock). To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of J-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. The pin header J-RTC is not stuffed on the SC9-TOCCATA by default.

NOTE: It is important to execute the RTC reset while the board has no power.

J-RTC	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	RTC reset performed

[1)] This setting is the factory default.

Connectors

This section describes pin-assignments of on-board connectors e.g. for mezzanine expansion, and CompactPCI® Serial backplane connectors.

Front panel connectors (3 x USB Type-C DP Alt Mode, 3 x RJ45 Ethernet) follow well known standards and can be used with ready assembled cables and adapters throughout available. The F/P connectors are therefore not described in detail in this section.

Caution

SC9-TOCCATA mezzanine connectors provide operating voltage (3.3V, 5V and 12V) to devices inside the system chassis, such as mezzanine cards or system internal peripherals. Not all of these power rails are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Power to external devices delivered by USB Type-C front panel receptacles is internally short circuit protected.

Mezzanine Connectors

Three connectors are available for SC9-TOCCATA mezzanine expansion. Two high speed signal connectors (HSE1, HSE2) and in addition a side band I/F connector (N-EXP) are populated on top of the CPU board.

EKF offers low profile mezzanine modules which fit into the 4HP envelope of the CPU carrier card, with varying B2B clearance from 10.0mm to 10.8mm, and also side cards for additional 4HP mounting pitch (8HP in total assembly, 18.7mm B2B). The female connector N-EXP is identically populated on carrier and mezzanine and requires a suitable pin header (stacker) as contact element between carrier and mezzanine in addition. The HSE1/HSE2 connectors of carrier and mezzanine are female (CPU) and male (mezzanine) pairs, selected to match the individual B2B height requirements:

HSE1/HSE2 Mezzanine Connectors	
Mezzanine Series, B2B	Connector
CPU Carrier	8mm female ERNI Microspeed 275.90.08.068.01
S2*, S4*, B2B 10.0mm	Supplement 2mm male connector for nominal height 10mm
S6*, S8*, B2B 10.8mm	Supplement 2mm male connector for nominal height 10mm
SC* side card, B2B 18.7mm	Supplement 8mm male connector for nominal height 18mm

The S8* mezzanines are intended to complement the CPU carrier card with respect to the P6 backplane connector, for up to 8 Gigabit Ethernet ports. The SC9-TOCCATA itself does not provide the P6 connector, according the CompactPCI® Serial Mezzanine Concept.

Series	Board to Board Space	HSE1	HSE2	M.2 Style	Type-C Front I/O	P6 Ethernet	Side Card Option 8HP (HSE2)
S2*	10.0mm	PCIe x4, USB3	1)	D3	✓	○	✓
S4*	10.0mm	PCIe x4, USB3	PCIe x4, DP	D3	✓	○	○
S6*	10.8mm	PCIe x4, USB3	1)	S3	○	✓	✓
S8*	10.8mm	PCIe x4, USB3	PCIe x4, DP	S3	○	✓	○

1) HSE2 recessed on mezzanine PCB - available for additional 8HP side card (option)

✓ Feasible (option)
○ Not scheduled or infeasible

D3 Double sided M.2 (top 1.5mm, bottom 1.35mm) or single sided M.2
S3 Single sided M.2 only (top 1.5mm)

HSE1 Mezzanine Connector

High Speed Expansion HSE1			
GND	a1	b1	GND
1_PCIE_TXP	a2	b2	3_PCIE_TXP
1_PCIE_TXN	a3	b3	3_PCIE_TXN
GND	a4	b4	GND
1_PCIE_RXN	a5	b5	3_PCIE_RXN
1_PCIE_RXP	a6	b6	3_PCIE_RXP
GND	a7	b7	GND
2_PCIE_TXP	a8	b8	4_PCIE_TXP
2_PCIE_TXN	a9	b9	4_PCIE_TXN
GND	a10	b10	GND
2_PCIE_RXN	a11	b11	4_PCIE_RXN
2_PCIE_RXP	a12	b12	4_PCIE_RXP
GND	a13	b13	GND
1_USB2_P	a14	b14	2_USB3_TXP
1_USB2_N	a15	b15	2_USB3_TXN
GND	a16	b16	GND
2_USB2_P	a17	b17	2_USB3_RXP
2_USB2_N	a18	b18	2_USB3_RXN
GND	a19	b19	GND
1_2_USB_OC#	a20	b20	PCIE_CLK_P
PLTRST#	a21	b21	PCIE_CLK_N
+3.3VS [1)]	a22	b22	+5VS [1)]
+3.3VS [1)]	a23	b23	+5VS [1)]
+3.3VA [3)]	a24	b24	+5VPS [2)]
+12VPS [2)]	a25	b25	+12VPS [2)]

1) Power rail switched on in S0 state only
2) Power rail switched on in S0-S4 state
3) Power always on

The HSE1 PCIe® lanes are derived from the Tiger Lake processor (Gen4 capable, fixed x4 link)

HSE2 Mezzanine Connector

High Speed Expansion P-HSE2			
1_PCIE_TXP	a1	b1	3_PCIE_TXP
1_PCIE_TXN	a2	b2	3_PCIE_TXN
GND	a3	b3	GND
1_PCIE_RXN	a4	b4	3_PCIE_RXN
1_PCIE_RXP	a5	b5	3_PCIE_RXP
GND	a6	b6	GND
2_PCIE_TXP	a7	b7	4_PCIE_TXP
2_PCIE_TXN	a8	b8	4_PCIE_TXN
GND	a9	b9	GND
2_PCIE_RXN	a10	b10	4_PCIE_RXN
2_PCIE_RXP	a11	b11	4_PCIE_RXP
GND	a12	b12	GND
DP_LANE0_P	a13	b13	DP_LANE2_P
DP_LANE0_N	a14	b14	DP_LANE2_N
GND	a15	b15	GND
DP_LANE1_P	a16	b16	DP_LANE3_P
DP_LANE1_N	a17	b17	DP_LANE3_N
GND	a18	b18	GND
PCIE_CLK_P	a19	b19	DP_AUX_P
PCIE_CLK_N	a20	b20	DP_AUX_N
GND	a21	b21	DP_CFG1
I2C_SCL [1)]	a22	b22	DP_HPD
I2C_SDA [1)]	a23	b23	PLTRST#
+12VPS [2)]	a24	b24	+12VPS [2)]
+12VPS [2)]	a25	b25	+12VPS [2)]

1) Connected to PCH I2C Bus Controller 0
2) Power rail switched on in S0-S4 state

The HSE2 PCIe® lanes are derived from the PCH (Gen3 capable, configurable link width)

N-EXP Mezzanine Connector

N-EXP • Next Gen Expansion Board Interface				
	GND	1	2	+3.3VS [1]
	eSPI_CLK	3	4	PLTRST#
	eSPI_IO[0]	5	6	eSPI_IO[1]
	eSPI_IO[2]	7	8	eSPI_IO[3]
	eSPI_CS0#	9	10	eSPI_RST#
	GND	11	12	+3.3VS [1]
	GPP_H23/TIME_SYNC0	13	14	eSPI_ALERT#
	PPM (TSN)	15	16	PPS (TSN)
	GPP_C13/UART2_TXD	17	18	GPP_C12/UART2_RXD
	GPP_B1/TIME_SYNC1	19	20	GPP_C14/UART2_RTS#
	GND	21	22	+5VS [1]
	GPP_C8/UART1_TXD	23	24	GPP_C10/UART1_RTS#
	GPP_C9/UART1_RXD	25	26	GPP_C11/UART1_CTS#
	GPP_C15/UART2_CTS#	27	28	RESET_IN# [4]
	EXP_SCL [3]	29	30	EXP_SDA [3]
	GND	31	32	+5VS [1]
	HDA_SDOUT	33	34	HDA_SDIN0
	HDA_RST#	35	36	HDA_SYNC
	HDA_BITCLK	37	38	VCC_RTC [5]
	SPEAKER	39	40	+12VPS [2]

pin orientation shows CPU carrier board top view

1) Power rail switched on in S0 state only
2) Power rail switched on in S0-S4 state
3) Connected to I2C controller 0 of PCH
4) Connected to the PLD reset logic to force hardware reset
5) Can be used as an alternate way to supply the RTC well

CompactPCI® Serial Backplane Connectors

The SC9-TOCCATA is provided with five high speed backplane connectors P1 - P5, compliant with the CompactPCI® Serial specification (pin mapping for system boards with respect to SC9-TOCCATA).

The PCI Express® links/lanes 1_PE_* to 2_PE_* are derived directly from the processor and theoretically capable to transfer 16GT/s (PCIe® Gen4). Since only Gen1-3 is specified for CompactPCI® Serial and the AirMax VS® backplane connectors J/P1-J/P6, the maximum Gen4 transfer rate cannot be guaranteed (depends e.g. on backplane characteristics and peripheral card). For details of the connectors please visit Amphenol-ICC (formerly FCI).

The SC9-TOCCATA is equipped with the new AirMax VSe® 25Gb/s differential pair backplane connectors for doubling the data transfer rate to PCIe® Gen4 (CompactPCI® Serial R3.0).

The 1_PE and 2_PE links are assigned via the backplane to the CompactPCI® Serial fat pipe slots, for a maximum link width of x8 each.

3_PE to 8_PE are 8GT/s (PCIe® Gen3) links. While the 3_PE link provides x4 support, the remaining links 4_PE to 8_PE are organized x1.

The CompactPCI® Serial connector pin assignment distinguishes positive/negative (+/-) PCIe® differential signals. However, polarity inversion may be used on several lanes for optimum PCB routing. This is allowed according the PCI Express® Base Specification and has no effect on function or performance of the respective link. The pin-out shown is as per specification.

If backplane Ethernet shall be supported, P6 is available as an option on a low profile mezzanine module (S8* series), with up to 8 ports (switch based) or 4 ports (NICs). A pin assignment for P6 is not part of this document. Instead, refer to the mezzanine modules Technical Information, e.g. https://www.ekf.com/s/s80/s80.html or https://www.ekf.com/s/s82/s82.html.

P1

P1 CompactPCI® Serial System Slot Backplane Connector Type A AirMax VSe® 72 pos. 12x6, 14mm Width												
P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1 PE TX02+	1 PE TX02-	GND	1 PE RX02+	1 PE RX02-	GND	1 PE TX03+	1 PE TX03-	GND	1 PE RX03+	1 PE RX03-
5	1 PE TX00+	1 PE TX00-	GND	1 PE RX00+	1 PE RX00-	GND	1 PE TX01+	1 PE TX01-	GND	1 PE RX01+	1 PE RX01-	GND
4	GND	1 USB2+	1 USB2-	GND	RSV	RSV	GND	1 SATA TX+	1 SATA TX-	GND	1 SATA RX+	1 SATA RX-
3	1 USB3 TX+	1 USB3 TX-	PWR BTN#	1 USB3 RX+	1 USB3 RX-	PWR_ FAIL#	SATA SDI 4) 5)	SATA SDO 3) 4)	GA2	SATA SCL 2) 4)	SATA SL 4)	GA3
2	GND	I2C SCL 7)	I2C SDA 7)	GND	PS_ ON#	RST#	GND	PRST#	WAKE_ IN#	GND	RSV	SYS EN# 6)
1	+12V	+5V STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed gray: not connected

2) This pin may carry the IEEE 1588 Pulse per Second (PPS) signal when enabled within UEFI/BIOS settings.
3) This pin may carry the IEEE 1588 Pulse per Minute (PPM) signal when enabled within UEFI/BIOS settings.
4) 10kÙ Pull-Up resistor to +3.3V when board is inserted in system controller slot.
5) This pin is connected to PCH GPIO GPP_F12
6) This pin is connected to PCH GPIO GPP_D17
7) These pins are connected to PCH I^2C Controller 1

P2

P2 CompactPCI® Serial Slot Backplane Connector Type B AirMax VSe® 96 pos. 12x8, 16mm Width												
P2	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	BPID SCL 1)	BPID SDA 1)	GND	2 USB2+	2 USB2-	GND	3 USB2+	3 USB2-	GND	4 USB2+	4 USB2-
7	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
6	GND	2 PE TX06+	2 PE TX06-	GND	2 PE RX06+	2 PE RX06-	GND	2 PE TX07+	2 PE TX07-	GND	2 PE RX07+	2 PE RX03-
5	2 PE TX04+	2 PE TX04-	GND	2 PE RX04+	2 PE RX04-	GND	2 PE TX05+	2 PE TX05-	GND	2 PE RX05+	2 PE RX05-	GND
4	GND	2 PE TX02+	2 PE TX02-	GND	2 PE RX02+	2 PE RX02-	GND	2 PE TX03+	2 PE TX03-	GND	2 PE RX03+	2 PE RX03-
3	2 PE TX00+	2 PE TX00-	GND	2 PE RX00+	2 PE RX00-	GND	2 PE TX01+	2 PE TX01-	GND	2 PE RX01+	2 PE RX01-	GND
2	GND	1 PE TX06+	1 PE TX06-	GND	1 PE RX06+	1 PE RX06-	GND	1 PE TX07+	1 PE TX07-	GND	1 PE RX07+	1 PE RX07-
1	1 PE TX04+	1 PE TX04-	GND	1 PE RX04+	1 PE RX04-	GND	1 PE TX05+	1 PE TX05-	GND	1 PE RX05+	1 PE RX05-	GND

pin positions printed gray: not connected

1) These signals are subject of CompactPCI® Serial R3.0 and connected to PCH I2C Controller 2

P3

P3 CompactPCI® Serial Slot Backplane Connector Type B AirMax VSe® 96 pos. 12x8, 16mm Width												
P3	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	7 SATA TX+	7 SATA TX-	GND	7 SATA RX+	7 SATA RX-	GND	8 SATA TX+	8 SATA TX-	GND	8 SATA RX+	8 SATA RX-
7	5 SATA TX+	5 SATA TX-	GND	5 SATA RX+	5 SATA RX-	GND	6 SATA TX+	6 SATA TX-	GND	6 SATA RX+	6 SATA RX-	GND
6	GND	3 SATA TX+	3 SATA TX-	GND	3 SATA RX+	3 SATA RX-	GND	4 SATA TX+	4 SATA TX-	GND	4 SATA RX+	4 SATA RX-
5	8 USB3 TX+	8 USB3 TX-	GND	8 USB3 RX+	8 USB3 RX-	GND	2 SATA TX+	2 SATA TX-	GND	2 SATA RX+	2 SATA RX-	GND
4	GND	6 USB3 TX+	6 USB3 TX-	GND	6 USB3 RX+	6 USB3 RX-	GND	7 USB3 TX+	7 USB3 TX-	GND	7 USB3 RX+	7 USB3 RX-
3	4 USB3 TX+	4 USB3 TX-	GND	4 USB3 RX+	4 USB3 RX-	GND	5 USB3 TX+	5 USB3 TX-	GND	5 USB3 RX+	5 USB3 RX-	GND
2	GND	2 USB3 TX+	2 USB3 TX-	GND	2 USB3 RX+	2 USB3 RX-	GND	3 USB3 TX+	3 USB3 TX-	GND	3 USB3 RX+	3 USB3 RX-
1	5 USB2+	5 USB2-	GND	6 USB2+	6 USB2-	GND	7 USB2+	7 USB2-	GND	8 USB2+	8 USB2-	GND

pin positions printed gray: not connected

P4

P4 CompactPCI® Serial Slot Backplane Connector Type B AirMax VSe® 96 pos. 12x8, 16mm Width												
P4	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	6 PE TX02+	6 PE TX02-	GND	6 PE RX02+	6 PE RX02-	GND	6 PE TX03+	6 PE TX03-	GND	6 PE RX03+	6 PE RX03-
7	6 PE TX00+	6 PE TX00-	GND	6 PE RX00+	6 PE RX00-	GND	6 PE TX01+	6 PE TX01-	GND	6 PE RX01+	6 PE RX01-	GND
6	GND	5 PE TX02+	5 PE TX02-	GND	5 PE RX02+	5 PE RX02-	GND	5 PE TX03+	5 PE TX03-	GND	5 PE RX03+	5 PE RX03-
5	5 PE TX00+	5 PE TX00-	GND	5 PE RX00+	5 PE RX00-	GND	5 PE TX01+	5 PE TX01-	GND	5 PE RX01+	5 PE RX01-	GND
4	GND	4 PE TX02+	4 PE TX02-	GND	4 PE RX02+	4 PE RX02-	GND	4 PE TX03+	4 PE TX03-	GND	4 PE RX03+	4 PE RX03-
3	4 PE TX00+	4 PE TX00-	GND	4 PE RX00+	4 PE RX00-	GND	4 PE TX01+	4 PE TX01-	GND	4 PE RX01+	4 PE RX01-	GND
2	GND	3 PE TX02+	3 PE TX02-	GND	3 PE RX02+	3 PE RX02-	GND	3 PE TX03+	3 PE TX03-	GND	3 PE RX03+	3 PE RX03-
1	3 PE TX00+	3 PE TX00-	GND	3 PE RX00+	3 PE RX00-	GND	3 PE TX01+	3 PE TX01-	GND	3 PE RX01+	3 PE RX01-	GND

pin positions printed gray: not connected

P5

P5 CompactPCI® Serial Slot Backplane Connector Type C AirMax VSe® 72 pos. 12x6, 12mm Width												
P5	A	B	C	D	E	F	G	H	I	J	K	L
6	5 PE CLKE#	5 PE CLK+	5 PE CLK-	6 PE CLKE#	6 PE CLK+	6 PE CLK-	7 PE CLKE#	7 PE CLK+	7 PE CLK-	8 PE CLKE#	8 PE CLK+	8 PE CLK-
5	1 PE CLK+	1 PE CLK-	1 PE CLKE#	2 PE CLK+	2 PE CLK-	2 PE CLKE#	3 PE CLK+	3 PE CLK-	3 PE CLKE#	4 PE CLK+	4 PE CLK-	4 PE CLKE#
4	GND	8 PE TX02+	8 PE TX02-	GND	8 PE RX02+	8 PE RX02-	GND	8 PE TX03+	8 PE TX03-	GND	8 PE RX03+	8 PE RX03-
3	8 PE TX00+	8 PE TX00-	GND	8 PE RX00+	8 PE RX00-	GND	8 PE TX01+	8 PE TX01-	GND	8 PE RX01+	8 PE RX01-	GND
2	GND	7 PE TX02+	7 PE TX02-	GND	7 PE RX02+	7 PE RX02-	GND	7 PE TX03+	7 PE TX03-	GND	7 PE RX03+	7 PE RX03-
1	7 PE TX00+	7 PE TX00-	GND	7 PE RX00+	7 PE RX00-	GND	7 PE TX01+	7 PE TX01-	GND	7 PE RX01+	7 PE RX01-	GND

pin positions printed gray: not connected

PCB Dimensions

Beyond All Limits:
EKF High Performance Embedded

Industrial Computers Made in Germany

boards. systems. solutions.

Document No. 10057 • 7 December 2023

EKF Elektronik GmbH
Philipp-Reis-Str. 4 (Haus 1)
Lilienthalstr. 2 (Haus 2)
59065 HAMM
Germany

Phone +49 (0)2381/6890-0
Fax +49 (0)2381/6890-90
Internet www.ekf.com
E-Mail sales@ekf.com