Technical Information

CCE-PUNK • I/O Companion Board

Document No. 2996 • Edition 8

2008-11

Contents

About this Manual

This manual is a short form description of the technical aspects of the CCE-PUNK, required for installation and system integration. It is intended for the very advanced user only.

Edition History

EKF Document	Ed.	Contents/*Changes*	Author	Date
Text # 2996 cce_tie.wpd	1	Technical Information CCE-PUNK English, Preliminary Edition	jj	25 July 2006
	2	Added illustration 'Assembly Drawing'	jj	15 September 2006
	3	Corrected table rear I/O connector J1 pin assignment: +5V USB now J1 C24 (was previously J1 C11 by error)	jj	19 January 2007
	4	Added photo CCD/CCE	jj	8 February 2007
	5	Changed mechanical drawing	jj	3 May 2007
	6	Rev.1 Update	mib	10 October 2007
	7	+12V supply by carrier board available	mib	26 March 2008
	8	Added photos C10 C17 C30	jj	27 November 2008

Related Documents

For a description of the CCD-CALYPSO CPU card, which acts as PCIe/LPC controller and carrier board with respect to the CCE-PUNK, please refer to the correspondent CPU user guide, available by download from http://www.ekf.com/c/ccpu/ccd/ccd_e.html.

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Intel, Pentium, Celeron, Pentium M, Core Duo: ® Intel
- ***CompactPCI*** : ® PICMG
- Windows 2000, Windows XP: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Specifications/Standards	
CompactPCI	PICMG 2.0 R3.0 Okt. 1999 (www.picmg.org)
PCI Local Bus	PCI 2.2/2.3/3.0 Standards (PCI SIG www.pcisig.com)
USB	Universal Serial Bus Revision 2.0 specification (www.usb.org/developers)
PCI Express	PCIe Base Spec. 1.1 and other (PCI SIG www.pcisig.com)
1394 FireWire	IEEE 1394a-2000 (standards.ieee.org)
CompactFlash	CF+ and CompactFlash Specification Revision 3.0 (www.compactflash.org)

CCE-PUNK Features

Feature Summary	
Form Factor	Single size Eurocard (160x100mm^2), needs 4HP (20.3mm) additional mounting space, typically delivered as a ready to use assembly unit including the CCD-CALYPSO providing a common 8HP front panel shared with the CPU board, mounting position right (on top of CPU board)
LPC Super-I/O [3] (SIO2)	LPC47B27x, parallel port, 2 serial ports, floppy drive controller port, PS/2 keyboard & mouse port, infrared port, MIDI/gameport, fan control ports, GPIOs, serial IRQs
Firmware Hub [3] (FWH2)	82802 generic device, 8Mbit Flash, LPC interface
1394a FireWire [3]	XIO2200A, PCIe to 1394a bridge, dual cable port 400Mbps (100/200/400)
Serial Transceivers [3]	ADM211 or equivalent, EIA/TIA-232E (RS-232E) 230kbps max.
Front Panel Connectors [1]	▸ 2 x FireWire Receptacles ▸ 2 x RS-232E male D-Sub COM port connectors ▸ 2 x USB connectors
On-Board Connectors [1]	PCI Express expansion interface (PCIe x 1), LPC expansion interface, IDE/ATA 40-pin header 2.54mm, IDE/ATA 44-pin header 2.00mm (2.5-inch on-board hard disk), socket for CompactFlash mezzanine module or 1.8-inch hard disk module, floppy disk ZIF socket 26-pos., 1394 power, 1394 GPIO, 2 x serial port TTL header (EKF CU-module), 2 x fan heatsink header (pulse width modulation), 2 x fan heatsink header (tacho generator), MIDI header, GPIO, reset, PS/2 KB/MS
Rear I/O Connectors [1]	▸ J1: IDE, PS/2 KB/MS, USB, gameport, reset ▸ J2: Serial1/COM-A, Serial2/COM-B, LPT, floppy disk, USB, GPIO, IRDA, MIDI, speaker, fan
On-Board Functions	Speaker
Mass Storage Options [2]	▸ Hard disk drive 2.5-inch optional on-board ▸ Mezzanine module with 1.8-inch hard disk drive ▸ CompactFlash mezzanine module optional on-board
Thermal Conditions [4] Environmental Conditions [4]	▸ Operating temperature: 0°C ... +70°C ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	tbd

[1] Not all of these connectors may be present or functional on your actual CCE-PUNK board. Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering.

[2] Options may be exclusive, i.e. not necessarily concurrently present. Ask EKF for special solutions if required.

[3] Silicon/function may not be present on your actual CCE-PUNK board. Assembly of components is highly custom specific. Discuss your needs with EKF before ordering.

[4] Hard disk option may require decrease

Short Description

Available as a mezzanine companion board to the CCD-CALYPSO CPU card, the CCE-PUNK is provided with high-speed communication channels such as FireWire and USB, and common legacy I/O ports as well. Interconnection between the CCE-PUNK I/O module and the CPU carrier board is achieved by several expansion connectors, which comprise the PCIe (PCI Express), LPC (Low Pin Count) and ATA/IDE interfaces.

As an option, the CCE-PUNK is available with a rugged on-board 2.5-inch hard disk drive (1.8-inch SSD/HDD as a mezzanine module).

The CCE-PUNK will be attached on top of the CPU board, and shares its front panel typically with the host CPU carrier board (8HP front panel width in total).

In addition to its front panel I/O connectors, the CCE-PUNK has been designed also for rear I/O and therefore requires a non-bussed single-slot P1/P2 backplane in addition to the CompactPCI bus. However, if front panel I/O is solely needed, the J1/J2 connectors may be omitted as an option.

CCD-CALYPSO CPU Board with CCE-PUNK Mezzanine Companion Module

The CCE-PUNK communicates with the host CPU by means of 3 expansion connectors: P1 (LPC), P21 (PATA/IDE), and P30 (PCI Express).

The LPC (Low Pin Count) is a multiplexed ISA bus, enabling the super-I/O controller chip to emulate the legacy I/O interfaces. Among these are the classic parallel (printer) and serial (COM) ports.

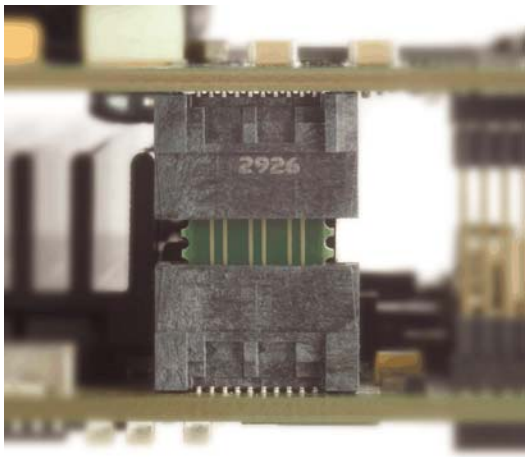
The Parallel ATA/IDE interface is still essential for embedded applications, due to the availability of ATA CompactFlash cards and 1.8-inch hard disks with an ATA/IDE compatible I/F only. Optionally, the CCE-PUNK can be equipped with either a CompactFlash mezzanine module, or a robust 2.5-inch hard disk drive, particularly suited for use in a rugged environment. A mezzanine module is also available which carries an 1.8-inch drive, as an alternative.

The CCE-PUNK fits on the top side of the CCD-CALYPSO CPU board, which is on the right side when looking at the front panel of the boards inserted into a CPCI rack.

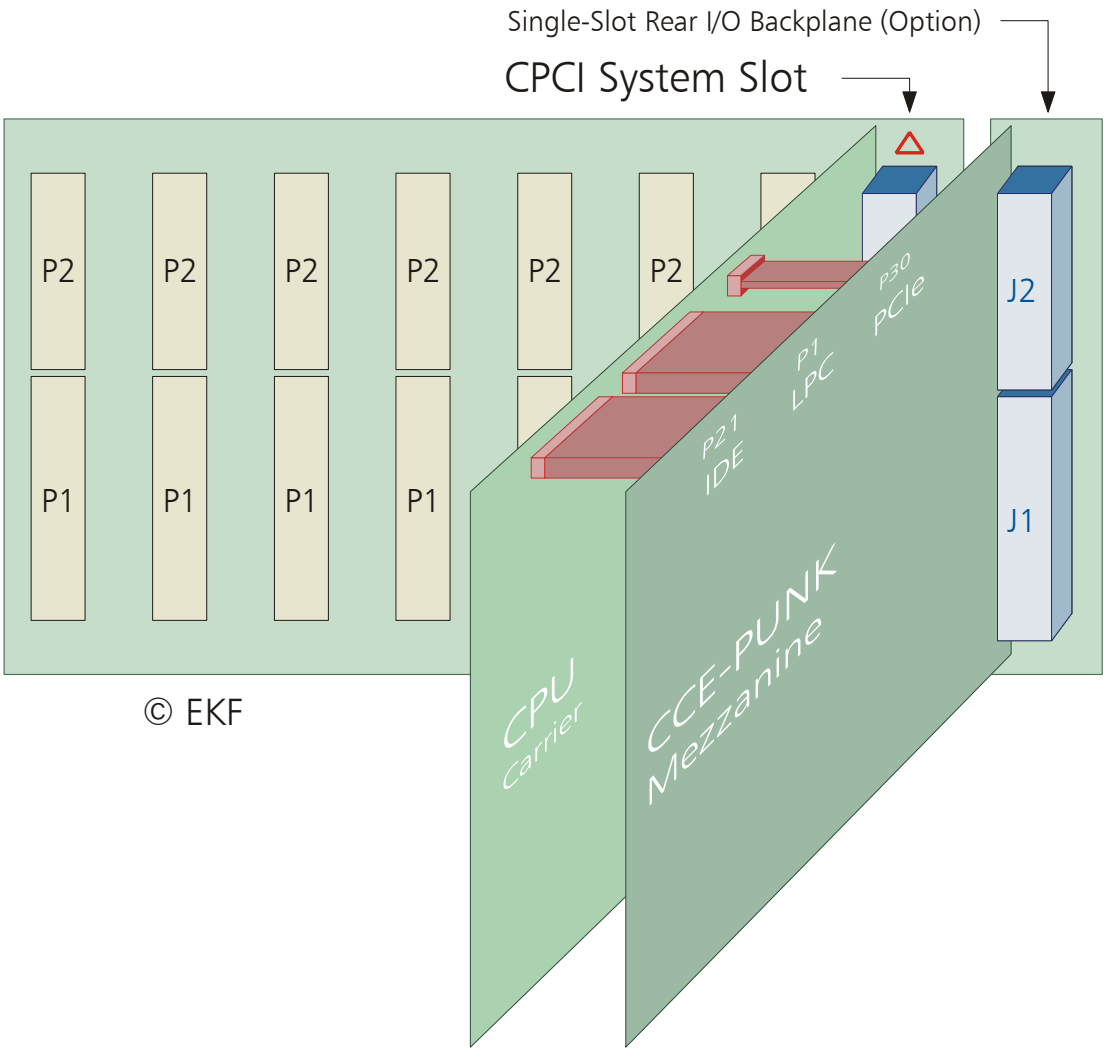
In addition to front panel I/O, some of the interfaces of the CCE-PUNK are available for rear I/O across the connectors J1/P1 and J2/P2. A suitable rear I/O transition module such as the CCZ-RIO would be required in addition to gain access to the I/O ports from the systems back panel.

Several I/O functions are also directly available by on-board headers on the CCE-PUNK, mainly the IDE interface. Other on-board connectors are only stuffed as an option, however.

If equipped with the rear I/O connectors J1/J2, the CCE-PUNK must be inserted on a slot outside of the CompactPCI backplane. A single slot rear I/O P1/P2 backplane should be present in the system rack at the CCE reserved slot. Most EKF systems have the CPCI busprint justified to the left margin of the 19-inch rack, with the system slot (CPU slot) orientated to the right end of the backplane. Following next to the right side, the CCE-PUNK should be placed in between the remaining free mounting space.



PCIe Board to Board Connectors



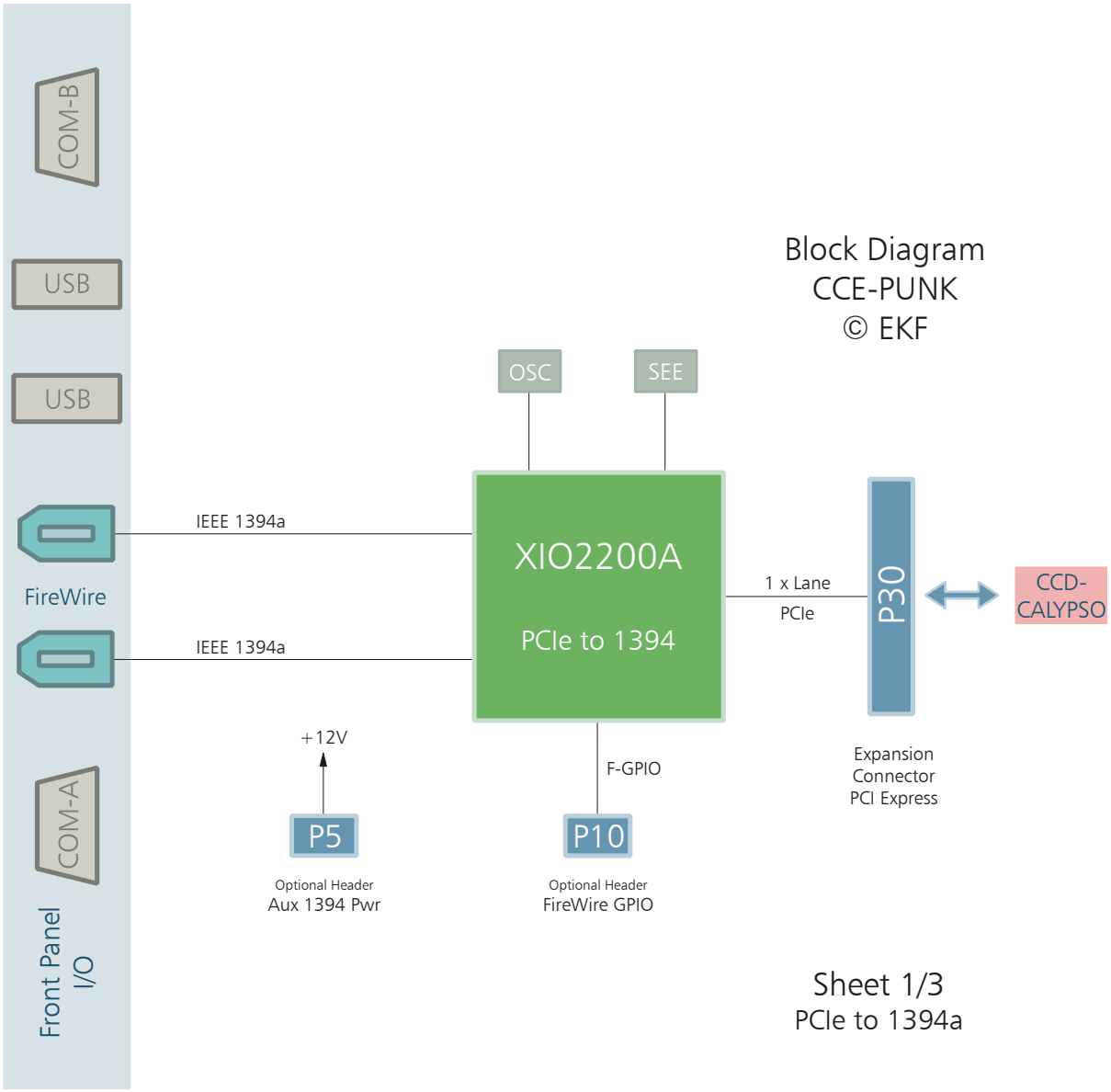
CCE-PUNK mounted on top of the CPU carrier board

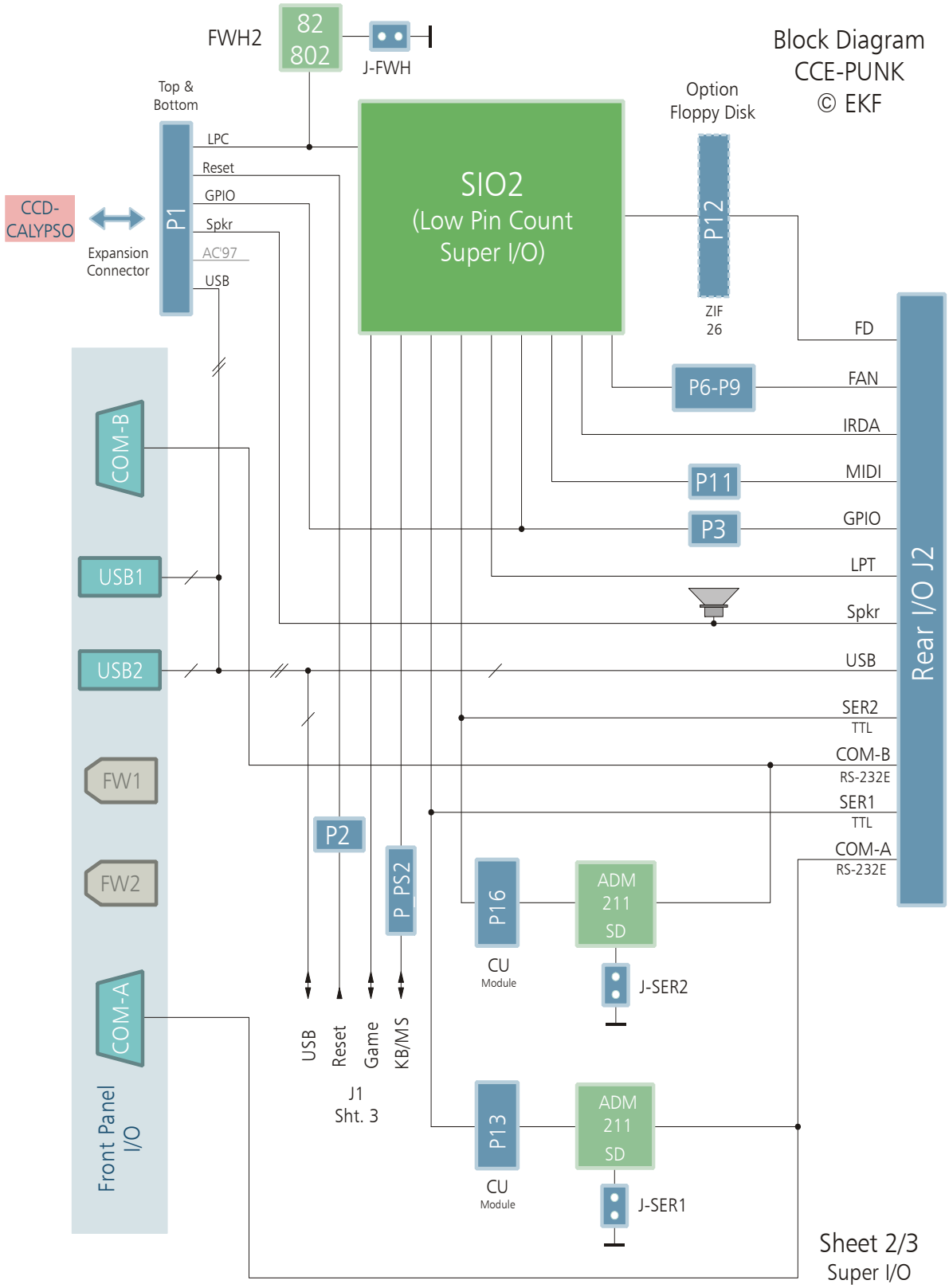
The suitable CPU carrier board for use together with the CCE-PUNK mezzanine module is the CCD-CALYPSO. The CCE-PUNK companion board mounts on top (at the right side) of the CCD-CALYPSO.

If the CompactPCI backplane is provided with a right aligned system slot, be sure to position the CPU carrier board to the rightmost CPCI slot (and not the CCE-PUNK). Consequently, The CCE-PUNK then occupies the next card slot to the right, outside of the CPCI backplane, which may be provided with a single slot rear I/O P1/P2 backplane. In order to make use of the rear I/O capability of the CCE-PUNK, its optional J1/J2 rear I/O connectors must be stuffed (consider before ordering). This assembly order (right aligned CPCI system slot) is preferred because no CompactPCI slot is lost for the CCE-PUNK.

Vice versa, if a CPCI backplane is mandatory with a left aligned system slot, the CCE-PUNK must not be equipped with J1/J2 connectors, and occupies a regular CompactPCI slot then. A coding key present on J1 would prevent insertion of the CCE-PUNK into a CPCI card slot. Of course, this assembly solution is not suitable for rear I/O of the CCE, and a CPCI slot will be lost.

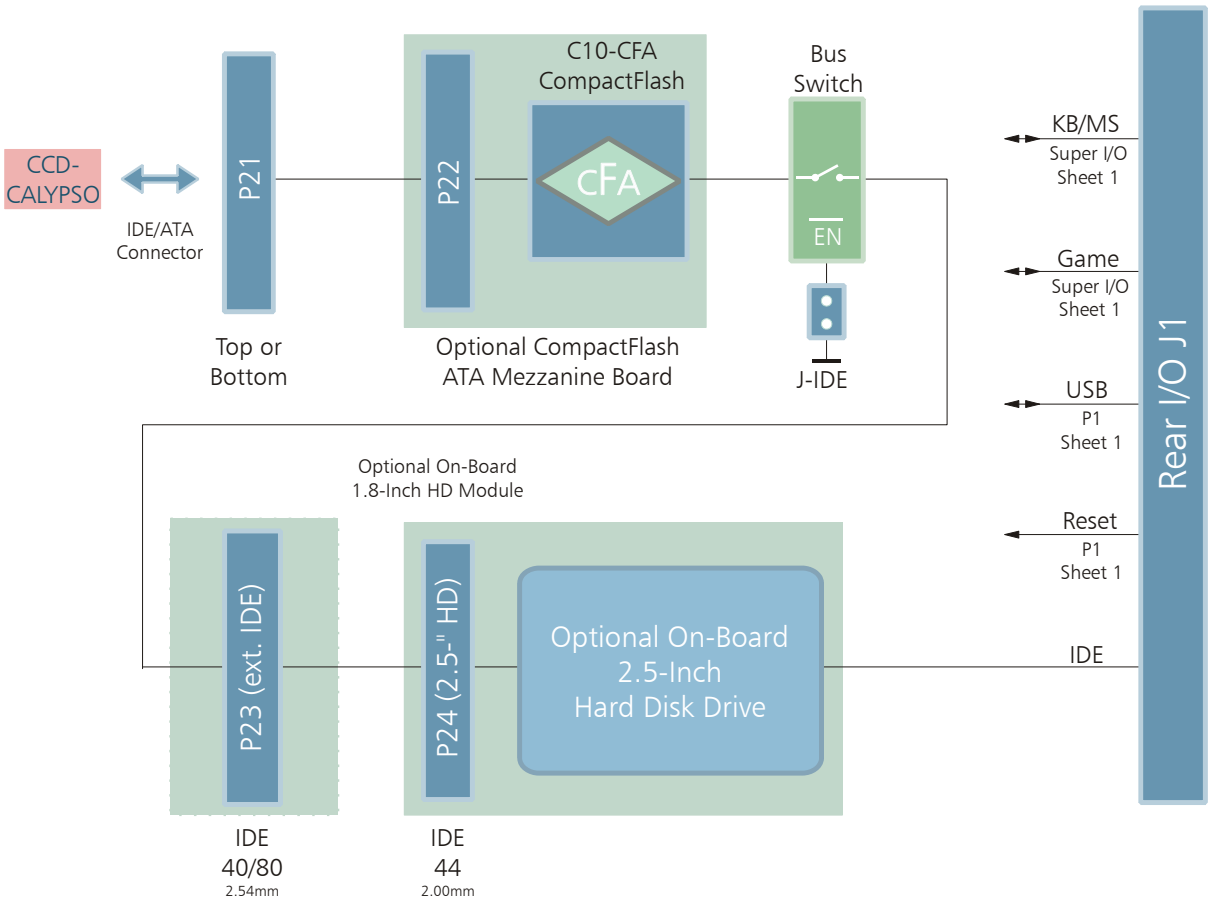
Block Diagram CCE-PUNK



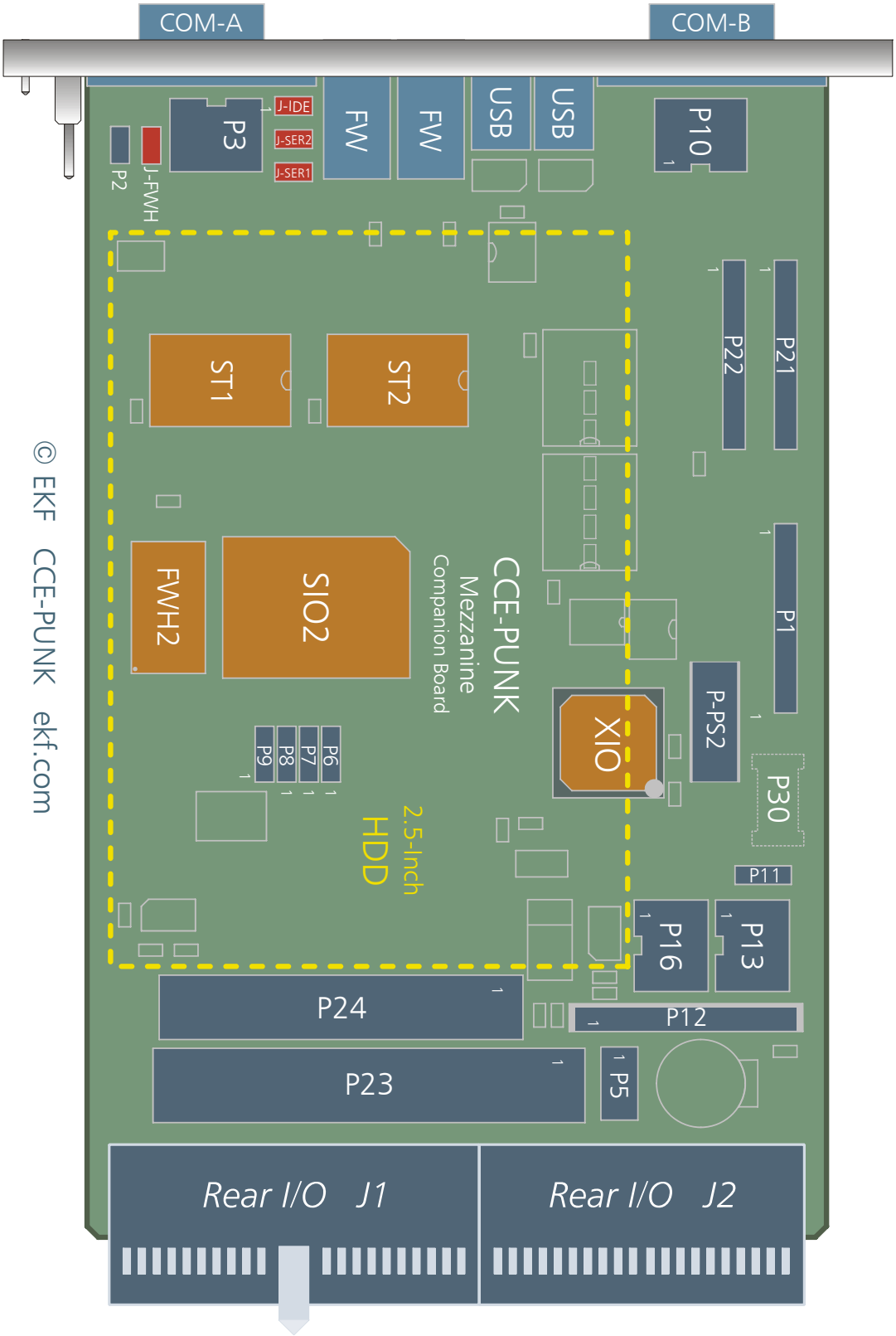

Block Diagram
CCE-PUNK
© EKF
FWH2
82 802
J-FWH
Top & Bottom
P1
LPC
Reset
GPIO
Spkr
AC'97
USB
CCD-CALYPSO
Expansion Connector
SIO2
(Low Pin Count Super I/O)
Option Floppy Disk
P12
ZIF 26
FD
P6-P9
FAN
IRDA
P11
MIDI
P3
GPIO
LPT
Spkr
USB
SER2
TTL
COM-B
RS-232E
SER1
TTL
COM-A
RS-232E
Rear I/O J2
COM-B
USB1
USB2
FW1
FW2
COM-A
Front Panel I/O
P2
P_PS2
USB
Reset
Game
KB/MS
J1
Sht. 3
P16
CU
Module
ADM 211 SD
J-SER2
P13
CU
Module
ADM 211 SD
J-SER1
Sheet 2/3
Super I/O

Block Diagram
CCE-PUNK
© EKF

Sheet 3/3
IDE Storage Options



Top View Component Assembly CCE-PUNK



On-Board Connectors

P1	Main (first) mezzanine expansion interface connector (dual row socket, normally available from bottom of the CCE-PUNK PCB, matching with the corresponding expansion interface socket on the CPU carrier board, connected through a board stacker), comprising of: • LPC Low Pin Count interface • AC'97 Audio Codec / HD Audio (Azalia) • 2 x USB • GPIO, Speaker, Reset
P2	Reset (hardware reset to the host CPU, pin header)
P3	GPIO General Purpose Inputs/Outputs pin header
P5	1394 Auxiliary power connector +12V
P6..P9	Fan heatsink pin headers
P10	XIO2200A (FireWire) GPIO pin header
P11	MIDI interface pin header
P12	Floppy disk header 26-pos. ZIF socket (slim-line drive)
P13	Serial port 1 (TTL level), pin header suitable for EKF CU-series PHY module
P16	Serial port 2 (TTL level), pin header suitable for EKF CU-series PHY module
P21	Second mezzanine expansion interface connector (dual row socket, normally available from bottom of the CCE-PUNK PCB, matching with the corresponding expansion interface socket on the CPU carrier board, connected through a board stacker), comprising of: • Host CPU (ICH6) IDE/ATA Interface
P22	Socket for C10-CFA CompactFlash adapter mezzanine module
P23	IDE 40-pin header for an external DVD drive or hard disk drive (3.5-inch), optionally to be used together with P10 drive power connector (future mezzanine modules)
P24	IDE 44-pin header for an on-board hard disk drive (2.5-inch)
P30	Third mezzanine expansion interface (high speed socket edge card connector, available from bottom of the CCE-PUNK PCB, matching with the corresponding expansion interface socket on the CPU carrier board, connected through a high speed PCB), comprising of: • PCI Express (PCIe) x 1 interface
P-PS2	PS/2 Keyboard / Mouse
J1	Rear I/O metric connector 5 x 25 brown key
J2	Rear I/O metric connector 5 x 22

Please note: Not all of these connectors may be present or functional on your actual CCE-PUNK board. Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering.

Front Panel Connectors

COM-A [1]	RS-232E serial communications port (CCE-PUNK on-board SIO2 serial port 1), D-Sub 9-position male connector
COM-B [1]	RS-232E serial port (CCE on-board SIO2 serial port 2), D-Sub 9-position male connector
FW1	1394a FireWire receptacle, PHY port 1
FW2	1394a FireWire receptacle, PHY port 2
USB1	USB type A root hub connector (CCD-CALYPSO USB1 port)
USB2	USB type A root hub connector (CCD-CALYPSO USB2 port)

[1] Due to a primary SIO which may be present on the CPU board itself, the BIOS may assign COM port numbers different from COM1/COM2 to these interface lines on the CCE-PUNK, e.g. COM2/COM3.

Jumpers

J-FWH [1]	Determines if the optional on-board firmware hub is acting as boot BIOS (jumper set) or as secondary BIOS (jumper removed = default).
J-IDE [1]	Enables IDE bus switches when set. Please note: In order to make use of either connector P23 (external IDE device), P24 (2.5-inch on-board hard disk) or rear I/O IDE across J1, the jumper J-IDE must be set. However, if neither P23..P24 nor J1 IDE is in use, J-IDE must be removed in order to avoid reflections on the IDE bus caused by tapped signal traces.
J-SER1 [1]	Enables the optional RS-232 transceiver (on-board SIO COM-A) when set. If removed, the transceiver is in a high-impedance shutdown mode. J-SER1 must be set in order to make use of the front panel connector COM-A.
J-SER2 [1]	Enables the optional RS-232 transceiver (on-board SIO COM-B) when set. If removed, the transceiver is in a high-impedance shutdown mode. J-SER2 must be set in order to make use of the front panel connector COM-B.

[1] Not all of these jumpers may be present or functional on your actual CCE-PUNK board. Assembly of these jumpers is highly custom specific. Discuss your needs with EKF before ordering.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Technical Reference - Connectors

Caution

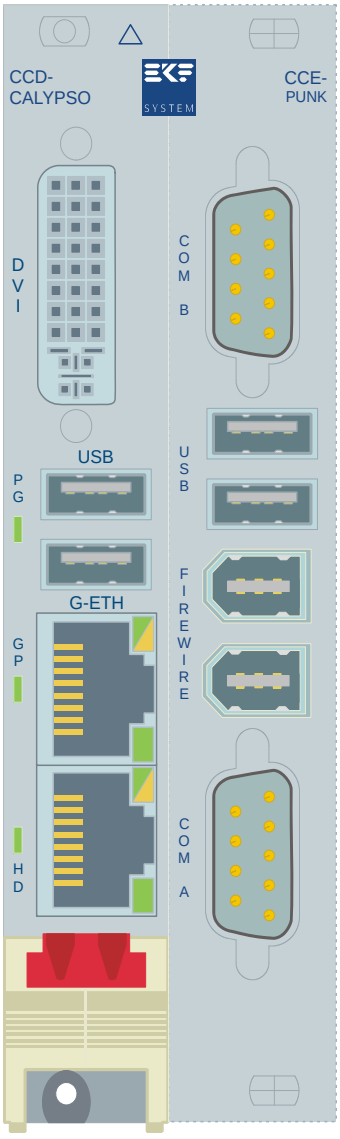
Some of the connectors provide operating voltage (e.g. +12V, +5V and +3.3V) to devices inside the system chassis, such as fans and internal peripherals. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Please Note

The CCE-PUNK transition module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the CCE board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order within the groups 'front panel connectors', 'on-board connectors', and 'rear I/O connectors').

Front Panel Connectors

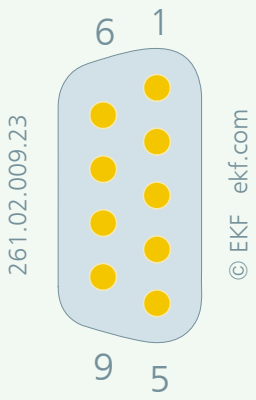
The suitable CPU carrier board for use together with the CCE-PUNK mezzanine module is the CCD-CALYPSO. The CCE-PUNK companion board mounts on top (at the right side) of the CCD-CALYPSO. By default, the CCE-PUNK shares an 8HP (~40.6mm) front panel with the CPU carrier board. Further more, custom specific front panel options are available on request.



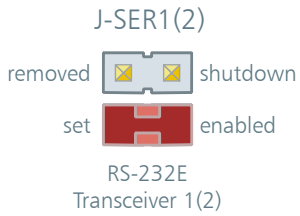
CCD-CALYPSO w. CCE-PUNK

COM-A/COM-B Serial Port Connectors

The on-board secondary Super-I/O (SIO) on the CCE-PUNK provides two asynchronous serial interfaces. Due to another (primary) SIO typically available on the CCD-CALYPSO host board, the serial interfaces are not necessarily dedicated to the COM-1/COM-2 ports of a typical PC. Verify or modify the accompanying CCD-CALYPSO BIOS settings for mapping of physical asynchronous serial I/O ports to the logical COM port order. Being ignorant of the actual port mapping, the serial port front panel connectors are marked neutrally as COM-A and COM-B.

COM-A/COM-B RS-232 Male D-Sub 9				
			1	DCD
	DSR	6		
			2	RXD
	RTS	7		
			3	TXD
	CTS	8		
			4	DTR
	RI	9		
			5	GND

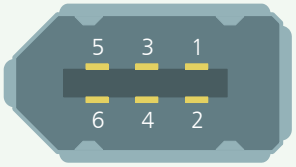
The on-board ESD protected RS-232E transceivers on the CCE-PUNK allow a bitrate of up to 230kbps. In order to make use of the front panel connectors COM-A and/or COM-B, the associated jumper(s) J-SER1 and/or J-SER2 must be set, which in turn enable(s) the associated transceiver(s). Please note that neither J-SER1 nor J-SER2 may be necessarily stuffed. A resistor combination may be present instead to simulate the jumpers.



The COM ports are alternatively also available across J2 as rear I/O communications interface. Be sure not to attach peripherals on both line endings simultaneously, the front panel connector and the rear I/O connector, which would result in interfering data.

1394 FireWire Connectors

The CCE-PUNK is equipped with an integrated PCIe to PCI bridge and 1394a OHCI compliant LLC/PHY (XIO2200A). Both cable port connectors are suitable for data transfer rates of 100Mbps, 200Mbps and 400Mbps according to IEEE1394a-2000.

1394a FireWire Receptacles		
 1394a FireWire Receptacle © EKF Part No. 270.30.06.1	1	+12V/0.5A Bus Power
	2	GND
	3	TP B-
	4	TP B+
	5	TP A-
	6	TP A+

The +12V is supplied by the carrier board. Using a CCD CPU board prior to rev.2, the cable port bus power (+12V) is present only if sourced across either

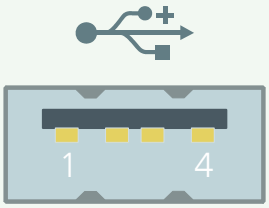
- the rear I/O connector J1 position 1D, or
- the auxiliary power connector P5 pin 4

If the application does not require 1394 cable port bus power, sourcing of +12V may be omitted.

Both cable ports are fused by an individual 0.5A PolySwitch. Due to a reasonable voltage drop across a Schottky diode, the actual bus power voltage is ~11.5V.

USB Connectors

The host CPU board CCD-CALYPSO is equipped with an ICH6 (Input/Output Controller Hub), which incorporates a number of USB 1.1/2.0 compliant ports. Two of the USB interfaces are routed to the CCE-PUNK mezzanine companion board across the expansion port connector P1. Normally both USB ports on the CCE-PUNK are available from the front panel.

USB Receptacles		
 270.20.04.1 © EKF	1	+5V_USB 0.5A 1)
	2	DATA-
	3	DATA+
	4	GND

1) Electronic Power Switch

As an alternative option to the front panel USB connectors, the CCE-PUNK may be stuffed for USB rear I/O of one or both USB interfaces across J1/J2. If this is the case, the corresponding front panel connector(s) would be either passivated, or may be removed (custom specific front panel).

On-Board Connectors

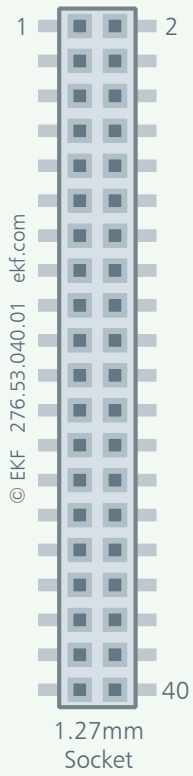
The CCE-PUNK can be equipped with several on-board connectors. Some of these connectors are available as an option only or exclusive to each other, and therefore may not be present on your actual board.

The expansion connectors P1, P21 and P30 are located on the bottom of the CCE-PUNK, for matching with the corresponding connectors of the CPU carrier board.

P1 and P21 can also be stuffed on top of the PCB, for attachment of the CCE-PUNK underneath the CCD-CALYPSO (option not available for P30 - FireWire ports not operational this way).

P1 Expansion Connector LPC/USB

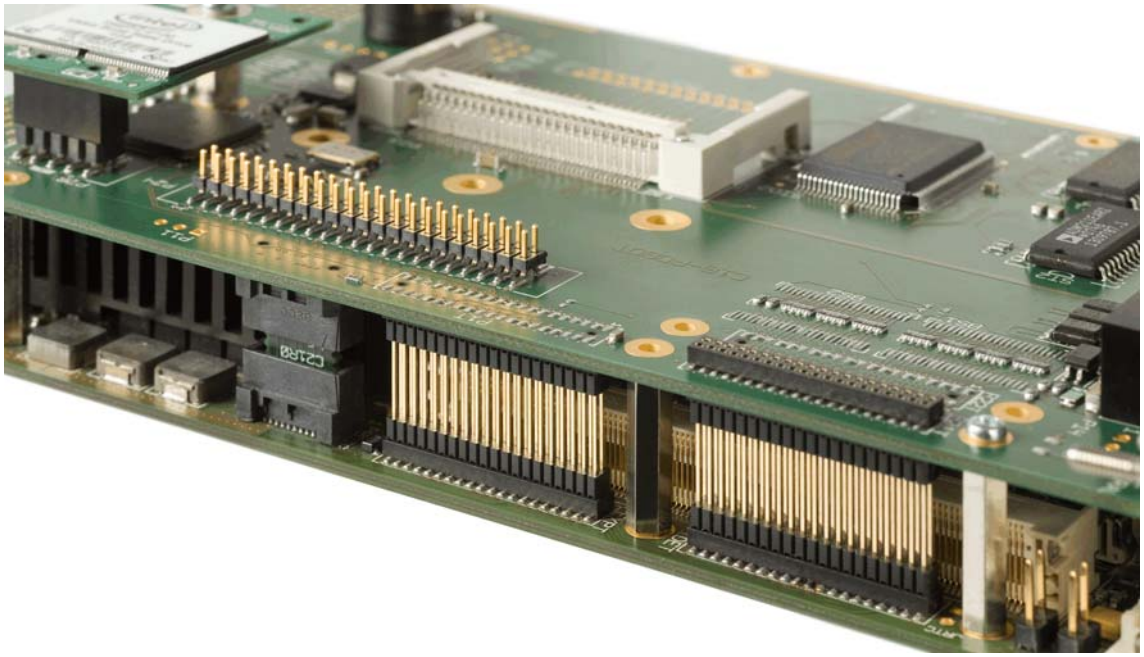
The expansion connector P1 is mounted on bottom of the CCE-PUNK PCB, with its face aligned towards the corresponding connector on the CCD-CALYPSO. This allows to attach the CCE-PUNK mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards. In addition to the other expansion connectors P21 (IDE) and P30 (PCI Express), P1 is used to pass the Low Pin Count I/F to the CCE-PUNK, besides USB channels and other sideband signals.



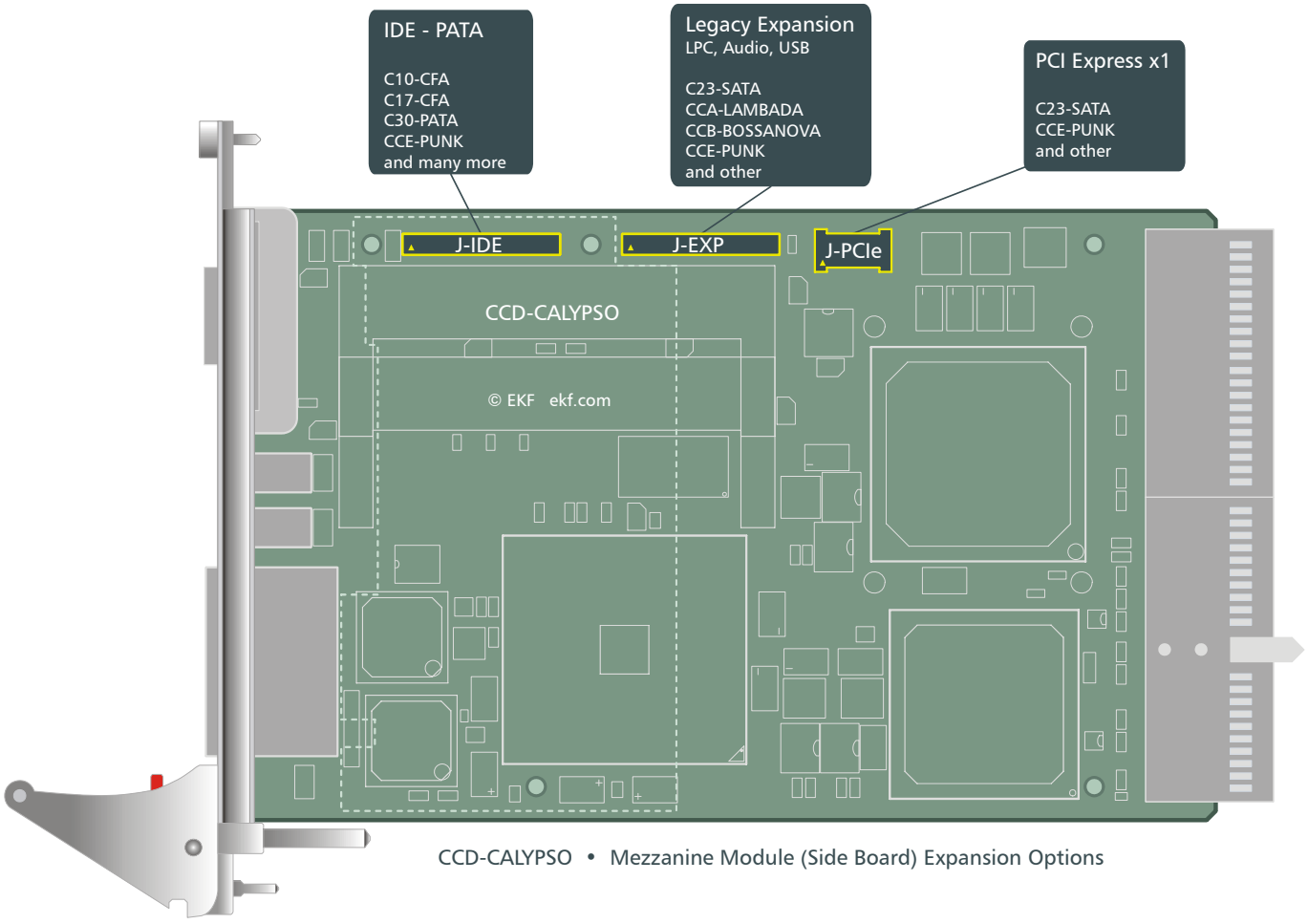
pin orientation shows
CPU carrier board top view

P1 Expansion Board Interface (LPC/AC'97/USB/GPIO) 1.27mm Socket 2 x 20			
GND	1	2	+3.3V
pciclk	3	4	pcirst#
lad0	5	6	lad1
lad2	7	8	lad3
lframe	9	10	ldrq#
GND	11	12	+3.3V
serirq	13	14	lpme#
lsmi#	15	16	sio_clk14
fwhid0	17	18	fwhinit#
kbrst#	19	20	a20gate
GND	21	22	+5V
usb2_d-	23	24	usb1_d-
usb2_d+	25	26	usb1_d+
usb_oc#	27	28	reset#
gp16	29	30	gp17
GND	31	32	+5V
ac_sdout	33	34	ac_sdin0
ac_rst	35	36	ac_sync
ac_bitclk	37	38	ac_sdin1
speaker	39	40	+12V [1) 2)]

[1)] CCD-CALYPSO rev. 2 or higher: This pin is connected to +12V via a 0-ohm jumper (default).
[2)] CCG-RUMBA: Unswitched power rail (switched on always).



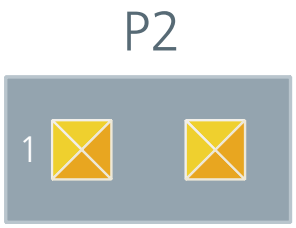
Mezzanine Connectors PCIe - Expansion - IDE



CCD-CALYPSO • Mezzanine Module (Side Board) Expansion Options

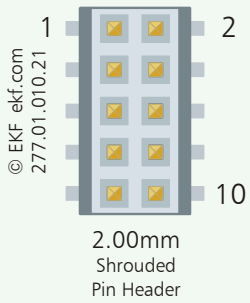
P2 Reset

Provided as an option, the pin header P2 can be used for resetting the CPU host board (processor reset) if wired to additional circuitry (e.g. watchdog or manual pushbutton). Tie reset# to GND with an open collector output.



P3 General Purpose Inputs/Outputs

The optional 2.00mm metric pin header P3 can be used for general purpose digital I/O. Please note, that these signals are also available for rear I/O on J2 - do not attach peripherals to both endings of a particular GPIO line. The GPI signals GPI1 and GPI2 are not 5V tolerant.

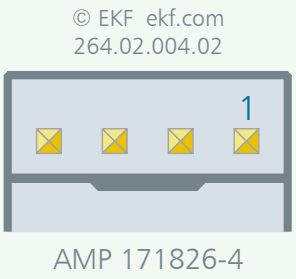
P3 GPIO 2.0mm Pin Header 2 x 5				
	GPI1 (on-Board FWH2) Input, 4.7k P/D 3.3V only - not 5V tol.	1	2	GPI2 (on-Board FWH2) Input, 4.7k P/D 3.3V only - not 5V tol.
	GPIO16 (CCD-CALYPSO SIO1) I/O, P/U 50K, 24mA, Input 5V tol.	3	4	GPIO17 (CCD-CALYPSO SIO1) I/O, P/U 50K, 24mA, Input 5V tol.
	GPIO21 (on-Board SIO2) I/O12, OD12, Input 5V tol.	5	6	GPIO22 (on-Board SIO2) I/O12, OD12, Input 5V tol.
	GPIO43 (on-Board SIO2) I/O8, OD8, Input 5V tol.	7	8	GPIO60 (on-Board SIO2) I/O12, OD12, Input 5V tol.
	GPIO61 (on-Board SIO2) I/O12, OD12, Input 5V tol.	9	10	GND

IO12	Input/Output, 12mA sink, 6mA source
OD12	Open Drain Output, 12mA sink
IO8	Input/Output, 8mA sink, 4mA source
OD8	Open Drain Output, 8mA sink

In addition, even more GPIO signals are available on P6..P9, P10, P11, P16..P17, J1, J2.

P5 Auxiliary Power Connector

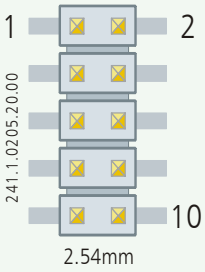
The optional floppy disk style power connector P5 may be used to supply the CCE-PUNK with +12V, concurrent with the carrier board and the optional J1 rear I/O connector. The 1394 bus power is derived from the +12V supply voltage (see also FireWire front panel connectors). A suitable cable assembly matching the AMP 171826-4 would be required (PC style power supplies typically provide a suitable strap for attachment of a floppy disk drive). Alternatively, P5 can be used to pass +5V redundantly (in addition to the expansion interface connector P1) to the CCE-PUNK, which can improve the power distribution when an on-board hard disk drive is in use (especially if a pair of drives is connected to P24). The current across P5 is limited by resettable fuses.

P5 Auxiliary Power		
	1	+5V_aux 1.5A
	2	GND
	3	GND
	4	+12V_aux 1.0A

Both voltages +5V and +12V are also available across the P1 onboard connector and the optional rear I/O connector J1. Usage of P5 is mainly a stopgap for systems with need for +12V, which cannot be equipped with a suitable rear I/O transition module. If the +12V rail is not at all required in a given application, neither P5 nor J1 are necessary for power distribution on the CCE-PUNK.

P-PS2

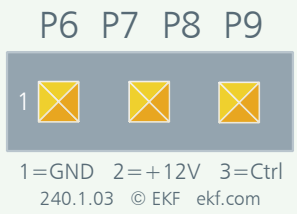
In most cases keyboard and mouse will be attached to the USB. As an option, the legacy PS/2 style signals are available from the pin header P-PS2. A cable harness or small adapter board is required for cross-over to the PS/2 Mini-Din female connector(s).

P-KM Keyboard - Mouse PS/2 Signals SMT 2.54mm Pin Header 2 x 5 (241.1.0205.20.00)				
	+5V Mouse [1]	1	2	Clock Mouse
	GND Mouse	3	4	Data Mouse
	NC	5	6	NC
	+5V Keyboard [1]	7	8	Clock Keyboard
	GND Keyboard	9	10	Data Keyboard

[1] short circuit protection by a common PolySwitch resettable fuse, voltage derived from +5V_CR carrier board switched power well

P6..P9 Cooling Fan Headers

The on-board SIO2 is provided with control ports for cooling fans with either a tachometer output (P6/P7) or PWM input (P8/P9). The benefit of a tachometer is to realize a fan operation failure, which would allow to punctual shutdown a system before a damage can occur. A fan with PWM input would allow to control the number of revolutions dependent from the CPU temperature, which can increase the lifetime of a fan considerably. The optional pin-headers P6..P9 may be used for attachment of suitable cooling fans.

P6 - P9 (2.54mm Pin Row)		
	1	GND
	2	+12V 2.5A (in total)
	3	Tachometer (P6/P7) Pulse Width Modulation (P8/P9)

If a +12V fan is supplied with power by either connector P6..P9, the CCE-PUNK on-board auxiliary power connector P5 may be used to derive +12V from an external power supply. +12V is also wired to the J1 rear I/O connector and to the P1 onboard connector concurrently (a custom specific rear I/O backplane is required for sourcing +12V across J1).

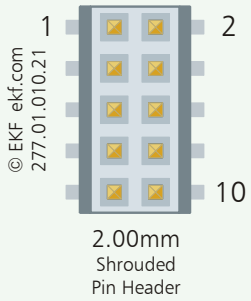
If P6..P9 are not required for fan control, the pins 3 of each header can be used as additional SIO2 GPIOs:

P6 Pin 3	GPIO30
P7 Pin 3	GPIO31
P8 Pin 3	GPIO32
P9 Pin 3	GPIO33

Since all fan control lines are as well available for rear I/O across J2, be sure to have connected any signal only once, in order to avoid interference.

P10 XIO2200 GPIO Connector

The optional 2.00mm metric pin header P10 may be used for general purpose digital I/O. The signals are derived from the 1394 FireWire controller XIO2200A. Please note, that these signals are not 5V tolerant.

P10 1394 GPIO 2.0mm Pin Header 2 x 5				
	GPIO0 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.	1	2	GPIO1 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.
	GPIO2 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.	3	4	GPIO3 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.
	GPIO6 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.	5	6	GPIO7 CMOS I/O, internal Pull-Up 3.3V only - not 5V tol.
	NC	7	8	NC
	+3.3V	9	10	GND

The signals GPIO4/5 are reserved for XIO2200A internal use (EEPROM I2C emulation).

In addition, even more GPIO signals are available on P3, P6..P9, P11, P16..P17, J1, J2.

P11 MIDI Header

As an option, a single row pin-header is stuffed, which provides MIDI I/O.

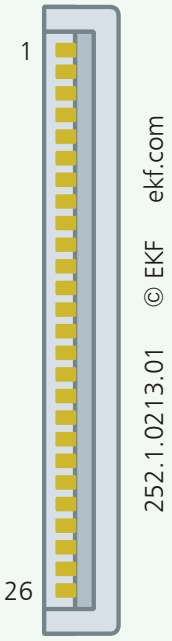
P11 MIDI 2.54mm Pin Header Single Row		
	1	MIDI-IN / GPIO25
	2	GND
	3	MIDI-OUT / GPIO26

MIDI I/O is also available across the J2 rear I/O connector. Be sure to have connected any signal only once, in order to avoid interference or damage.

In addition to the MIDI I/F also dual joystick support is available through J1 rear I/O.

MIDI and joystick lines may be used as GPIO signals instead.

P12 Micro Floppy Disc Connector



1mm pitch
FFC/FPC receptacle
vertical ZIF 26-position

1) Fused by PolySwitch 1.5A

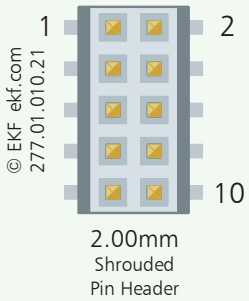
P12 Slim Line Floppy Disk 1mm ZIF Receptacle	
1	+5V_FDS 1)
2	index#
3	+5V_FDS 1)
4	ds0#
5	+5V_FDS 1)
6	dskchg#
7	NC
8	NC
9	drvden0#
10	mtr0#
11	NC
12	dir#
13	modsel
14	step#
15	GND
16	wdata#
17	GND
18	wgate#
19	GND
20	trk0#
21	NC
22	wrtprt#
23	GND
24	rdata#
25	GND
26	hdsel#

Optionally, the CCE-PUNK may be provided with a 26-position FFC/FPC ZIF socket, suitable for attachment of a single floppy disk drive with mating connector (typically low profile drives, e.g. TEAC FD05HF5630, Y-E Data YD-702J-6637, Citizen X1DE-00R, Mitsumi D353F3, Samsung SFD-321S, NEC FD1238H).

P13/P16 Serial Port 1/2 CU-Module Header

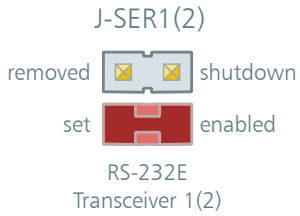
The on-board SIO2 is provided with two asynchronous serial interfaces. For attachment of EKF CU-series PHY modules via a micro ribbon flat cable assembly, the CCE-PUNK is optionally equipped with suitable pin-headers. A PHY module is a transceiver from TTL level signals to a specific symmetric or asymmetric interface standard, e.g. EIA-485 or RS-232E, with or w/o galvanic isolation. Usage of a PHY module requires that the associated on-board RS-232 transceiver is either disabled (J-SER1/2 removed) or not stuffed.

P13 & P16 Serial I/O CU-Module Standard 2.00mm Pin Header 2 x 5



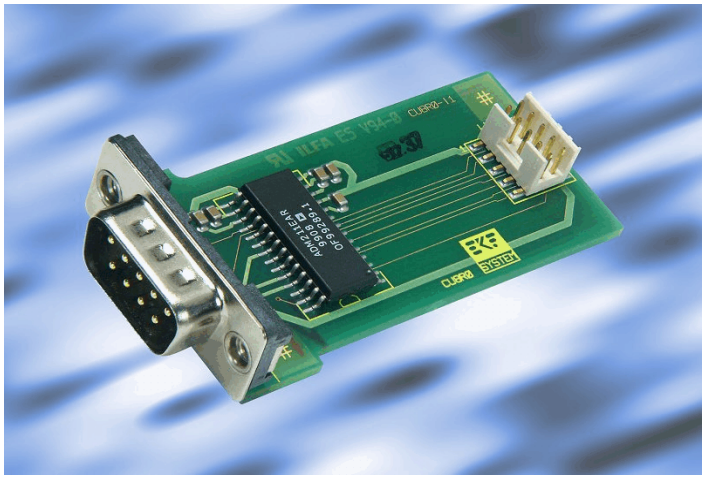
1) fused by PolySwitch

+5V_SER1(2) 0.5A 1)	1	2	DSR1(2)# / GPIO54 / IRQ9
RI1(2)# / GPIO50 / IRQ3	3	4	RXD1(2) / GPIO52 / IRQ5
TXD1(2) / GPIO53 / IRQ7	5	6	DTR1(2)# / GPIO57 / IRQ15
RTS1(2)# / GPIO55 / IRQ10	7	8	CTS1(2)# / GPIO56 / IRQ11
DCD1(2)# / GPIO51 / IRQ4	9	10	GND



The triple function shown in the table above (GPIO or IRQ in addition to the UART) is available solely for the serial port 2 (P16).

Since all signal lines are as well available for rear I/O across J2, be sure to have connected any signal only once, in order to avoid interference or damage.



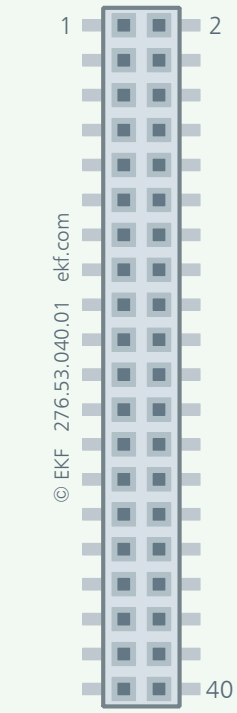
CU-Series PHY Module

P21/P22 IDE Expansion Connector & CompactFlash Mezzanine Connector

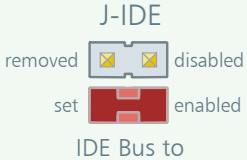
The expansion connector P21 is mounted on bottom of the CCE-PUNK PCB, with its face aligned towards the corresponding connector on the CCD-CALYPSO. This allows to attach the CCE-PUNK mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards. In addition to the expansion interface connector P1, which incorporates mainly the LPC interface, and P30 (PCI Express), P21 is dedicated to the ATA/IDE channel of the ICH6 (Input/Output Controller Hub) on the host CPU board.

The optional connector P22 is mounted on top of the CCE-PUNK and identical to P21and may be used as a replicator for a mezzanine module with a CompactFlash socket (EKF C10-CFA, part of the CCD-CALYPSO) or an 1.8-inch SSD/HDD mezzanine module (C30-PATA).

P21 & P22 CompactFlash/IDE Expansion Interface 1.27mm Socket 2 x 20



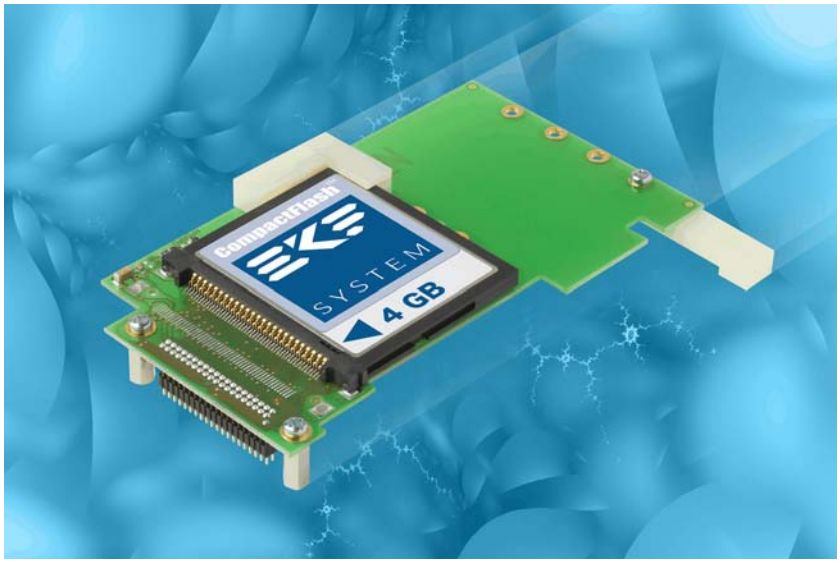
top view pin numbering order



IDE Bus to
P23 P24 J1

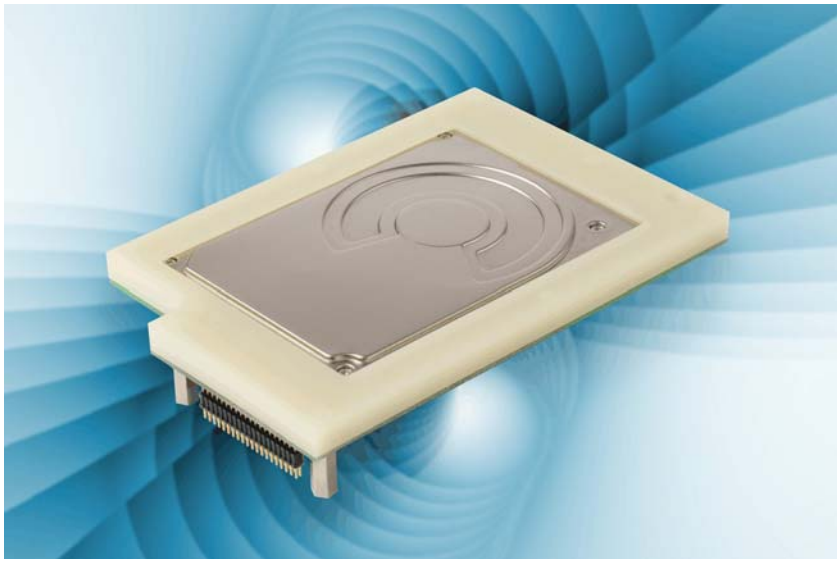
ide0_reset#	1	2	GND
ide0_dd07	3	4	ide0_dd08
ide0_dd06	5	6	ide0_dd09
ide0_dd05	7	8	ide0_dd10
ide0_dd04	9	10	ide0_dd11
ide0_dd03	11	12	ide0_dd12
ide0_dd02	13	14	ide0_dd13
ide0_dd01	15	16	ide0_dd14
ide0_dd00	17	18	ide0_dd15
GND	19	20	+3.3V
ide0_dmarq	21	22	+3.3V
ide0_diow#	23	24	GND
ide0_dior#	25	26	GND
ide0_iordy	27	28	+5V
ide0_dmack#	29	30	+5V
ide0_intrq	31	32	GND
ide0_da1	33	34	ide0_cblid#
ide0_da0	35	36	ide0_da2
ide0_cs1#	37	38	ide0_cs3#
ide0_act#	39	40	GND

If the CompactFlash adapter module is the only IDE device on the CCE-PUNK and no rear I/O IDE is required, the IDE signal lines to all other IDE connectors P23, P24 and J1 should be interrupted (remove jumper J-IDE, which in turn disables an electronic bus switch). This helps to avoid reflections on the IDE bus, which could otherwise degrade the signal quality.



C10-CFA (Top Mount)

C17-CFA (Bottom Mount)

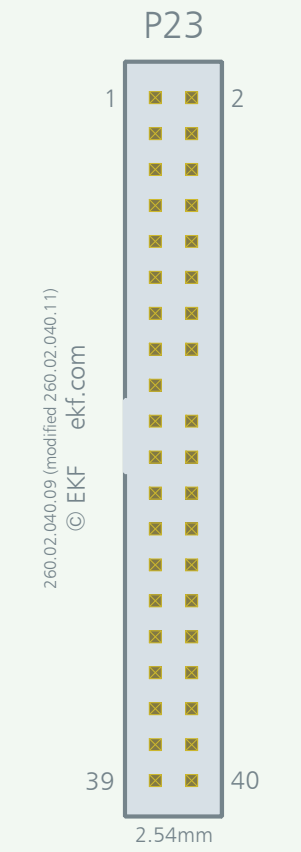


C30-PATA 1.8-Inch SSD (Top Mount)

P23 External IDE Header

P23 is provided optionally for attachment of classic IDE devices (e.g. 3.5-inch hard disk drive, DVD-ROM).

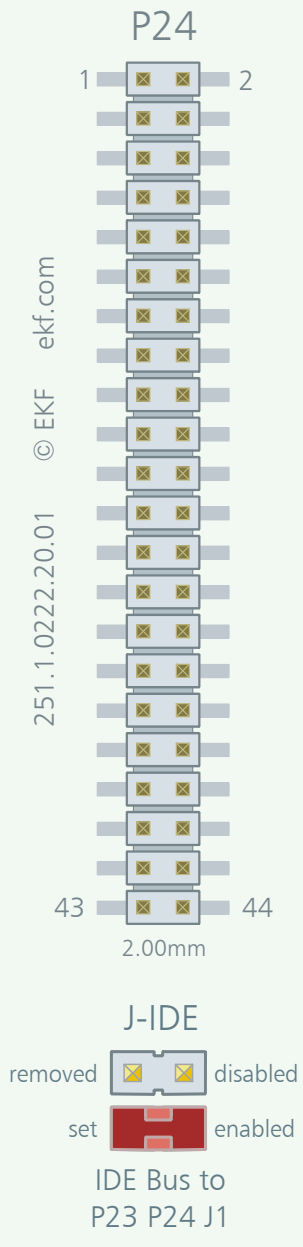
Usage of the IDE connector P23 requires the IDE bus switches enabled (jumper J-IDE set). No stubs are allowed on an IDE cable assembly, i.e. concurrent operation of devices attached to P23 and other IDE dedicated connectors cannot be guaranteed.



P23 External IDE Device 2.54mm Dual Row Pin Header			
ide1_reset#	1	2	GND
ide1_dd07	3	4	ide1_dd08
ide1_dd06	5	6	ide1_dd09
ide1_dd05	7	8	ide1_dd10
ide1_dd04	9	10	ide1_dd11
ide1_dd03	11	12	ide1_dd12
ide1_dd02	13	14	ide1_dd13
ide1_dd01	15	16	ide1_dd14
ide1_dd00	17	18	ide1_dd15
GND	19	*20*	KEY
ide1_dmarq	21	22	GND
ide1_diow#	23	24	GND
ide1_dior#	25	26	GND
ide1_iordy	27	28	GND
ide1_dmack#	29	30	GND
ide1_intrq	31	32	NC
ide1_a1	33	34	ide1_cblid#
ide1_a0	35	36	ide1_da2
ide1_cs1#	37	38	ide1_cs3#
ide0_act#	39	40	GND

P24 IDE/ATA Connector for 2.5-Inch Drives

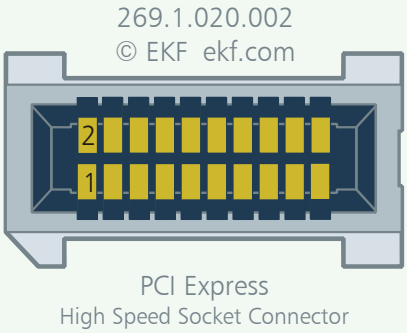
P24 is optionally provided for a 2.5-inch on-board hard disk drive. Usage of P24 requires the IDE bus switches enabled (jumper J-IDE set). No stubs are allowed on an IDE cable assembly, i.e. concurrent operation of devices attached to P24 and other IDE dedicated connectors cannot be guaranteed.



P24 On-Board 2.5-Inch Hard Disk Drive 2.00mm Pin Header 2x22			
ide1_reset#	1	2	GND
ide1_dd07	3	4	ide1_dd08
ide1_dd06	5	6	ide1_dd09
ide1_dd05	7	8	ide1_dd10
ide1_dd04	9	10	ide1_dd11
ide1_dd03	11	12	ide1_dd12
ide1_dd02	13	14	ide1_dd13
ide1_dd01	15	16	ide1_dd14
ide1_dd00	17	18	ide1_dd15
GND	19	*20*	KEY
ide1_dmarq	21	22	GND
ide1_diow#	23	24	GND
ide1_dior#	25	26	GND
ide1_iordy	27	28	GND
ide1_dmack#	29	30	GND
ide1_intrq	31	32	NC
ide1_da1	33	34	ide1_cblid#
ide1_da0	35	36	ide1_da2
ide1_cs1#	37	38	ide1_cs3#
ide0_act#	39	40	GND
+5V_HD	41	42	+5V_HD
GND	43	44	NC

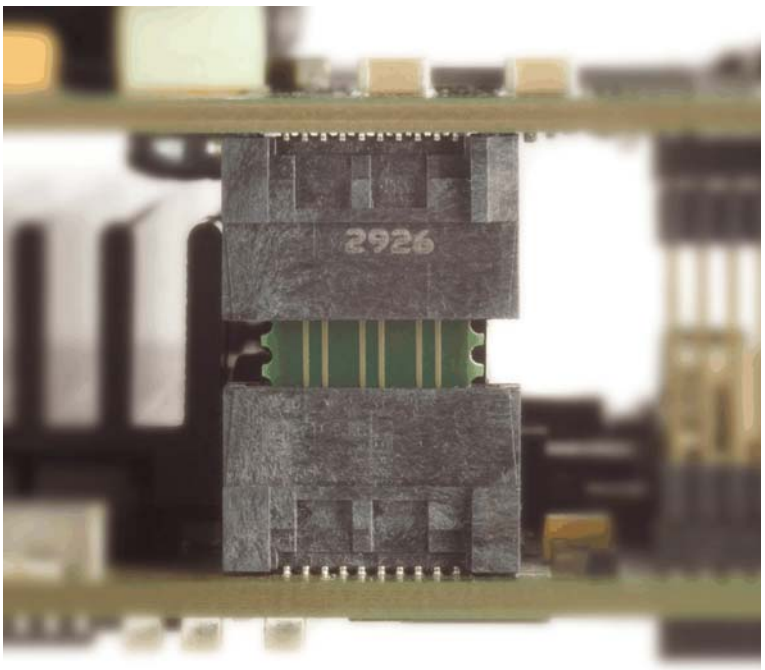
P30 PCI Express Connector

The high speed expansion connector P30 is mounted on bottom of the CCE-PUNK PCB, with its face aligned towards the corresponding connector on the CCD-CALYPSO. This allows to attach the CCE-PUNK mezzanine companion card on top of the CPU carrier board. A strip line PCB is used in addition to bridge the gap between the two boards. In addition to the expansion interface connectors P1 and P21, which incorporate the LPC and IDE interfaces, P30 is used as PCIe x 1 Lane.



pin orientation shows
CPU carrier board top view

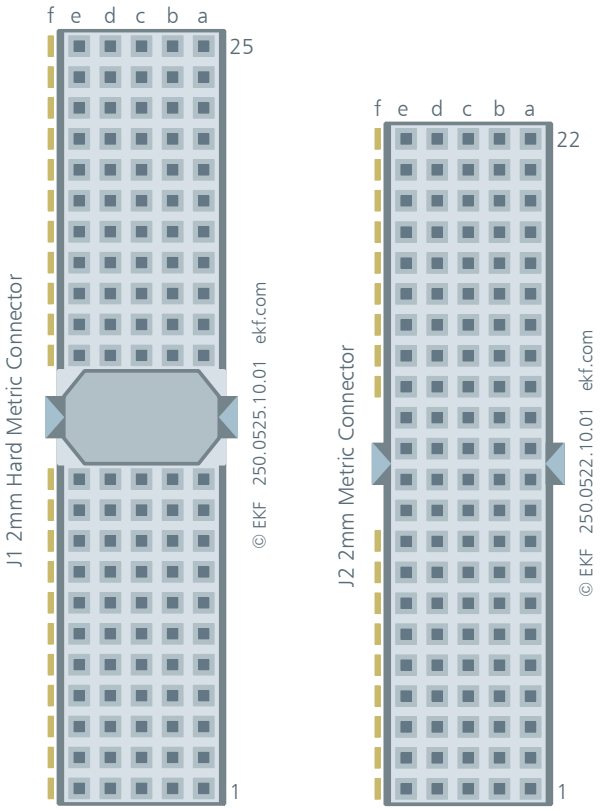
P30 PCI Express x 1 High Speed Dual Row Socket 0.8mm Pitch			
GND	1	2	GND
+5V	3	4	+3.3V
+5V	5	6	+3.3V
GND	7	8	GND
PE_CLKP	9	10	PE_RST#
PE_CLKN	11	12	PE_WAKE#
GND	13	14	GND
PE_1TP	15	16	PE_1RP
PE_1TN	17	18	PE_1RN
GND	19	20	GND



J1/J2 Rear I/O

As an option, the CCE-PUNK can be equipped with the rear I/O connectors J1 and J2. A single slot rear I/O backplane (directly adjoining the CPCI backplane) would be required for handing over the available signal lines to a suitable rear I/O transition module.

The CCE-PUNK must not be plugged into a common CPCI slot in order to avoid damaging the board or other components of the system. A brown key on the J1 connector will prevent the user from erroneously inserting the CCE-PUNK into an unsuitable position.



Signal names provided on the J1 and J2 connector tables hereafter are associated with their main function. However, the Super I/O controller allows a number of signals also be used as general purpose I/O. Please consult the SMSC LPC47B27x datasheet for details (www.smsc.com).

Please note, that the majority of signals is also available on-board or via front panel. Be sure to have connected any signal only once, in order to avoid interference.

With respect to the IDE/ATA interface, the jumper J-IDE (if provided) must be set, in order to enable rear I/O mass storage attachment. No stubs are allowed on an IDE cable assembly, i.e. concurrent operation of devices attached to J1 and other IDE dedicated connectors cannot be guaranteed.

J1 Rear I/O Connector

#J1	A	B	C	D	E
25	+5V	USB5_d+	USB5_d-	+3.3V	+5V
24	IDE_d08	+5V	+5V_USB5 VI/O	IDE_reset#	IDE_d07
23	+3.3V	IDE_d09	IDE_d10	+5V	IDE_d06
22	IDE_d11	GND	+3.3V	IDE_d04	IDE_d05
21	+3.3V	IDE_d12	IDE_d13	M66EN (GND)	IDE_d03
20	IDE_d14	GND	VI/O	IDE_d01	IDE_d02
19	+3.3V	IDE_d15	IDE_dmarq	GND	IDE_d00
18	IDE_dmack#	GND	+3.3V	IDE_ior#	IDE_iow#
17	+3.3V	IDE_a1	IDE_cblid#	GND	IDE_iordy
16	IDE_a2	GND	VI/O	IDE_a0	IDE_intrq
15	+3.3V	IDE_cs1#	IDE_act#	GND	IDE_cs0#
14					
13			KEY (BROWN)		
12					
11				GND	KB_dat
10		GND	+3.3V		KB_clk
9				GND	MS_dat
8		GND	VI/O		MS_clk
7				GND	+5V_PS2
6		GND	+3.3V	GPI1	GPI2
5				GND	
4	dbreset#	GND	VI/O	GP16	GP17
3	GAME_but21	GAME_but22	GAME_joy2x	+5V	GAME_joy2y
2	GAME_but11	+5V	GAME_but12	GAME_joy1x	GAME_joy1y
1	+5V	-12V	keylock#	+12V	+5V

pin positions coloured gray: not connected

J2 Rear I/O Connector

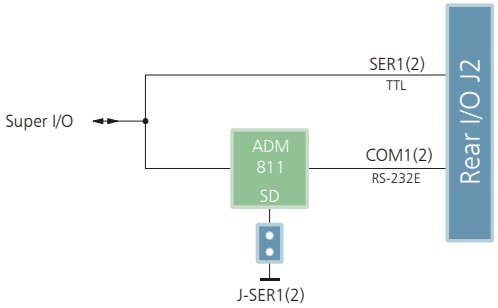
#J2	A	B	C	D	E
22	GPIO21	GPIO22	GPIO43	GPIO60	GPIO61
21	COM-A_ri	GND	COM-B_ri	COM-B_cts	FD_drvden0#
20	COM-A_cts	GND	COM-B_rxd	GND	FD_drvden1#
19	GND	GND	COM-B_dsr	COM-B_dcd	FD_index#
18	COM-A_rxd	COM-A_dsr	COM-B_dtr	GND	FD_mtr0#
17	COM-A_dcd	GND	COM-B_rts	COM-B_txd	FD_ds0#
16	COM-A_dtr	COM-A_rts	SER2_ri	GND	FD_dir#
15	COM-A_txd	GND	SER2_cts	SER2_rxd	FD_step#
14	SER1_ri	SER1_cts	SER2_dsr	GND	FD_wdata#
13	SER1_rxd	GND	V(I/O)	SER2_dcd	FD_wgate#
12	SER1_dsr	SER1_dcd	SER2_dtr	GND	FD_trk0#
11	SER1_dtr	GND	V(I/O)	SER2_rts	FD_wrtprt#
10	SER1_rts	SER1_txd	SER2_txd	GND	FD_rdata#
9	SER1_shdn	GND	V(I/O)	SER2_shdn	FD_hdsel#
8	LPT_slct	LPT_pe	LPT_busy	GND	FD_dskchg#
7	LPT_ack#	GND	V(I/O)	USB6_d+	USB6_d-
6	LPT_d7	LPT_d6	LPT_d5	GND	+5V_USB6
5	LPT_d4	GND	V(I/O)	MIDI_out	MIDI_in
4	V(I/O)	LPT_d3	LPT_slctin#	GND	speaker
3	LPT_d2	GND	LPT_init#	IRDA_tx	IRDA_rx
2	LPT_d1	LPT_error#	LPT_d0	FAN_tach2	FAN_tach1
1	LPT_alf#	GND	LPT_strobe#	FAN_pwm2	FAN_pwm1

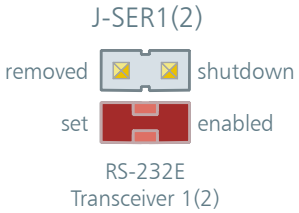
pin positions coloured gray: not connected

RS-232E Transceivers

The Super-I/O chip provides two asynchronous serial ports (TTL level), which are passed via the J2 rear I/O connector to a rear I/O transition module (option).

Furthermore, the CCE-PUNK is optionally provided with two serial transceivers according to RS-232E. As with the TTL level serial port signals, also the RS-232 transmission lines are wired to the J2 rear I/O connector for usage on a transition module (back panel COM port connectors). Each transceiver can be individually disabled by the jumpers J-SER1 and J-SER2, if either the particular RS-232 interface is not at all required (with a power saving effect), or if a different interface type is required, e.g. EIA/TIA-485 or optically isolated RS-232 (physical transceivers attached to the TTL level signals, located either on the rear I/O transition module, or attached to P13/P16).



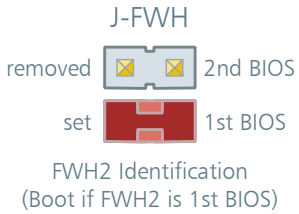


Conclusion: Each on-board transceiver on the CCE-PUNK must be enabled by setting its associated jumper J-SERx in order to use the COMx rear panel connector(s). If however the serial TTL lines are needed for a special interface solution, the particular on-board transceiver(s) must be disabled by removing its jumper J-SERx.

CU-Series PHY Module

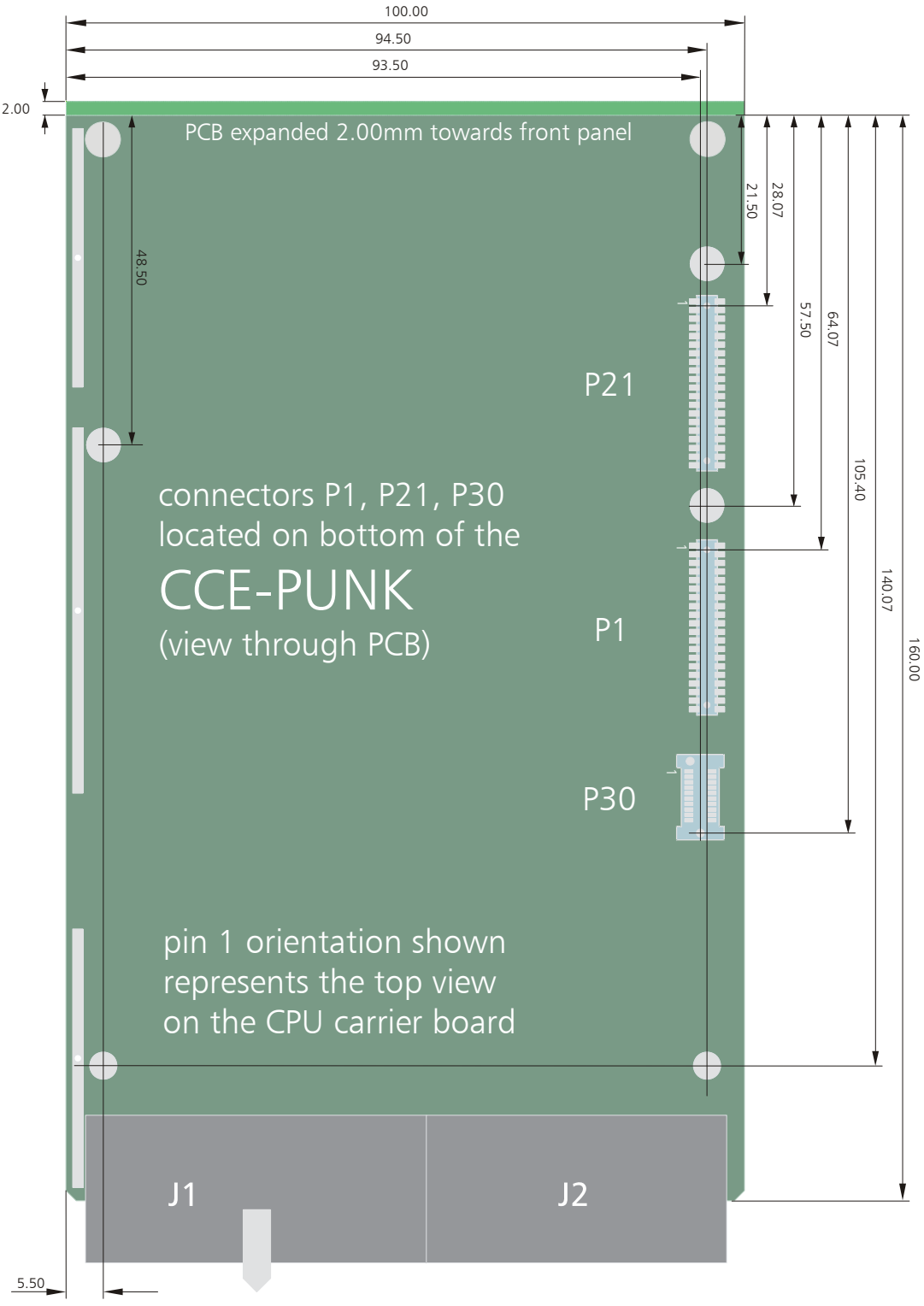
Firmware Hub 2

The CCE-PUNK is optionally provided with a 82802 compatible 8Mbit Flash (Firmware Hub), which can be used either as alternative boot BIOS, as an expansion memory to the CPU board BIOS, or for BIOS retrieval/rescue. The Firmware Hub is connected to the LPC (Low Pin Count) interface. The device ID of a particular FWH determines whether it is detected as BIOS after power on (ID = 0). If stuffed, the jumper J-FWH sets the on-board FWH2 ID to zero (and simultaneously changes the CCD-CALYPSO FWH ID to 1) - hence the system will use the BIOS on the CCE-PUNK after power-on.



A programming tool for the Firmware Hub and latest BIOS releases can be obtained from the EKF website.

Mechanical Drawing Expansion Connectors



Schematics

Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact sales@ekf.de for details.

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