SYSTEM

Technical Information

CCL-CAPELLA

Mezzanine I/O Expansion Board

Quad Gigabit Ethernet Networking Controller

Document No. 5124 • Ed. 5 • 2009-11

Contents

About this Manual

This manual is a short form description of the technical aspects of the CCL-CAPELLA, required for installation and system integration. It is intended for the advanced user only.

Edition History

EKF Document	Ed.	Contents/*Changes*	Author	Date
Text # 5124 ccl_tie.wpd	1	Technical Information CCL-CAPELLA English, Preliminary Edition	jj	7 April 2008
	2	Changed Block Diagram, reflecting secondary SATA controller silicon	jj	23 October 2008
	3	PCI Express packet switch silicon changed, P-SP3 and P-SP4 have been replaced by P-SP1 and P-SP2, board revision 1	jj	11 November 2008
	4	Added Images CCL	jj	5 January 2009
	5	Added photos C20-SATA	jj	13 November 2009

Related Documents

For a description of the CCG-RUMBA and CCM-BOOGIE CPU cards, which act as carrier boards with respect to the CCL-CAPELLA, please refer to the correspondent CPU user guide, available by download from www.ekf.com/c/ccpu/ccg/ccg_e.html or www.ekf.com/c/ccpu/ccm/ccm_e.html (change path accordingly for other possible CPU carrier boards).

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Intel, Pentium, Celeron, Core 2 Duo, Merom, Penryn, iAMT: ® Intel
- Santa Rosa Platform, Crestline Chipset GM965: Intel
- Montevina Platform, Cantiga Chipset GS45: Intel
- ***CompactPCI®*** : ® PICMG
- Windows 2000, Windows XP, Windows Vista: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Specifications/Standards	
CompactPCI	PICMG 2.0 (www.picmg.org)
PCI Local Bus	PCI 2.2/2.3/3.0 Standards (PCI SIG www.pcisig.com)
PCI Express	PCIe Base Spec. 1.1 and other (PCI SIG www.pcisig.com)
Ethernet	IEEE 802.3 (standards.ieee.org)
SATA	Serial ATA 2.5/2.6 Specification (www.sata-io.org)
FireWire	IEEE 1394a-2000 (standards.ieee.org)
USB	Universal Serial Bus Revision 2.0 specification (www.usb.org/developers)
TPM	Trusted Platform Module 1.2 (https://www.trustedcomputinggroup.org)

CCL-CAPELLA Features

Feature Summary	
Form Factor	Single size Eurocard (160x100mm^2), needs 4HP (20.3mm) mounting space in addition to CPU carrier board, typically delivered as a ready to use assembly unit (including the CCG-RUMBA or successor CPU card), provided with a common 8HP front panel shared with the CPU board, mounting position right (on top of CPU board)
PCIe Packet Switch PCIe Usage	▸ PCIe packet switch 12 ports, 12 lanes ▸ 4 Lanes (configured as 1 link x 4 lanes) to host (carrier board ICH) ▸ 4 Lanes individually assigned to 4 Gigabit Ethernet NICs ▸ 1 Lane dedicated to 1394a FireWire Controller ▸ 1 Lane dedicated to SATA/PATA controller
Gigabit Ethernet Networking Interface Controller (NIC) [3]	▸ 4 ports, each equipped with the Intel 82574L (Hartwell), 82574IT on request (extended temperature range), low power integrated MAC+PHY ▸ Copper standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab) ▸ PCI Express 2.5GHz ▸ Supports 9018-byte jumbo packets ▸ 40KB packet buffer size ▸ TimeSync Offload compliant with 802.1as specification ▸ Front panel access, or J1 rear I/O, individually configurable (BIOS setup) for each port ▸ Intel driver and diagnostics software
FireWire Controller [3]	▸ PCI Express integrated LLC/PHY XIO2200A ▸ Fully compliant with IEEE 1394a-2000 and 1394-1995 ▸ Fully compliant with 1394 Open Host Controller Interface (OHCI) Spec ▸ Two cable ports 400Mbps (200/100), 1 front panel receptacle, 1 rear I/O
SATA/PATA [3]	▸ JMB363 PCIe to 2 x SATA II / 1 x PATA controller ▸ JMB362 PCIe to 2 x SATA II controller ▸ RAID level 0/1 capable, drivers RAID or non-RAID ▸ Three options of SATA usage: C20-SATA mezzanine module (P-SATA1), rear I/O (J1), or standard SATA connectors (P-SATA2 & P-SATA3)
LPC Super-I/O [3] (SIO2)	▸ SCH3114, parallel port, 4 serial ports, PS/2 keyboard & mouse port, GPIO (all available via rear I/O J2 connector) ▸ Alternatively two serial ports available on-board (P-SER3 & P-SER4) for attachment of EKF CU-series PHY modules
Firmware Hub [3] (FWH2)	82802 generic device, 8Mbit Flash, LPC interface, can be configured (jumper) as secondary or primary (boot code) FWH
TPM [3]	Option Trusted Platform Module cryptographic chip according to TPM 1.2
Front Panel Connectors [1]	▸ 4 x RJ45 Ethernet (10/100/1G) jacks with integrated status LEDs ▸ 1 x IEEE 1394a FireWire receptacle
Host I/F Connectors (to CPU Carrier) [1]	▸ PCI Express interface (PCIe x 4) ▸ Multifunction expansion interface (LPC, USB, SMB)
On-Board I/O Connectors [1]	▸ Connector for mounting of optional C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch (RAID capable), high speed connector P-SATA1 ▸ 2 x Latched SATA headers 7-pos. (option), P-SATA2 & P-SATA3 ▸ Sockets for C17-CFA CompactFlash mezzanine module (bottom mount) or C30-PATA SSD mezzanine module (top mount) ▸ Up to 2 headers suitable for USB Solid State Drive (SSD) module (top & bottom mount) ▸ 2 x Serial port headers (TTL-level) P-SER3 & P-SER4 ▸ Reset

Rear I/O Connector Option [1]	Optional J1/J2 2.0mm hard metric connectors (CompactPCI style with proprietary signal mapping) for custom specific transition module or backplane, major signal groups: ▸ Parallel Port (LPT) ▸ COM ports 1 - 4 (TTL-level UART signals) ▸ PS/2 keyboard & mouse ▸ GPIO ▸ SMBus ▸ Ethernet rear I/O option ▸ SATA rear I/O option ▸ USB rear I/O option
On-Board Functions	Speaker, LEDs, SMBus EEPROM, temperature sensors
Mass Storage Options [2]	▸ C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch ▸ Up to 2 external SATA drives optionally attached to SATA headers ▸ Rear I/O SATA option ▸ C17-CFA (bottom mount) CompactFlash module ▸ C30-PATA (top mount) 1.8-inch SSD or HDD module ▸ USB Solid State Drive (SSD) module option (top and/or bottom mount)
Thermal Conditions [4] Environmental Conditions [4]	▸ Operating temperature: 0°C ... +70°C ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	tbd

[1] Not all of these connectors may be present or functional on your actual CCL-CAPELLA board. Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering.

[2] Options may be exclusive, i.e. not necessarily concurrently present. Ask EKF for special solutions if required.

[3] Silicon/function may not be present on your actual CCL-CAPELLA board. Assembly of components is highly custom specific. Discuss your needs with EKF before ordering.

[4] Hard disk option may require decrease

Short Description

Available as a mezzanine add-on expansion board to the CCG-RUMBA and successor CPU cards, the CCL-CAPELLA provides a number of additional I/O functions. First of all, the CCL-CAPELLA is a powerful Ethernet networking machine, with up to four independent low power Gigabit Ethernet controllers. Each GbE port can be individually routed either to a front panel jack, or the rear I/O connector, by software controlled switches (BIOS setup).

The additional SATA/PATA controllers are useful for attachment of mass-storage devices, either on-board mounted, or externally (by cable or via rear I/O).

The optional FireWire ports are practical e.g. for vision systems with mixed 1394a and GbE type cameras, and is especially useful for quality-of-service demanding and isochronous applications.

Furthermore the CCL-CAPELLA is equipped with a SIO, which provides legacy I/O ports, such as serial, parallel, KB/MS (all available across rear I/O). A secondary Firmware Hub can be configured as alternate- or backup-BIOS. Another option available is the Trusted Platform Module according to TPM 1.2 for safety critical applications.

The CCL-CAPELLA will be attached on top of the CPU carrier board, and typically shares its front panel with the host carrier (usually 8HP front panel width in total). Interconnection between the CCL-CAPELLA I/O module and the CPU carrier board is achieved by two expansion connectors, which comprise the PCIe (PCI Express x 4) and LPC (Low Pin Count) interfaces.

As an option, the CCL-CAPELLA is available with a mezzanine module (C20-SATA), which accommodates one or two 2.5-inch SATA hard disk drives (RAID option). Additionally, a CompactFlash card adapter (C17-CFA) can be mounted on bottom of the CCL-CAPELLA. As an alternative, a top mount 1.8-inch storage module (C30-PATA) is available, for HDD or SSD usage. As another option, up to two USB Flash drive modules can be accommodated, top and bottom.

The CCL-CAPELLA is best suited for demanding networking I/O applications, e.g. routers, gateways, vision systems, or network fabric. Maximum throughput is achieved through PCI Express technology. Combined with the two GbE ports available on the CPU carrier board, six individual networking interfaces altogether are provided for high performance Ethernet communication.

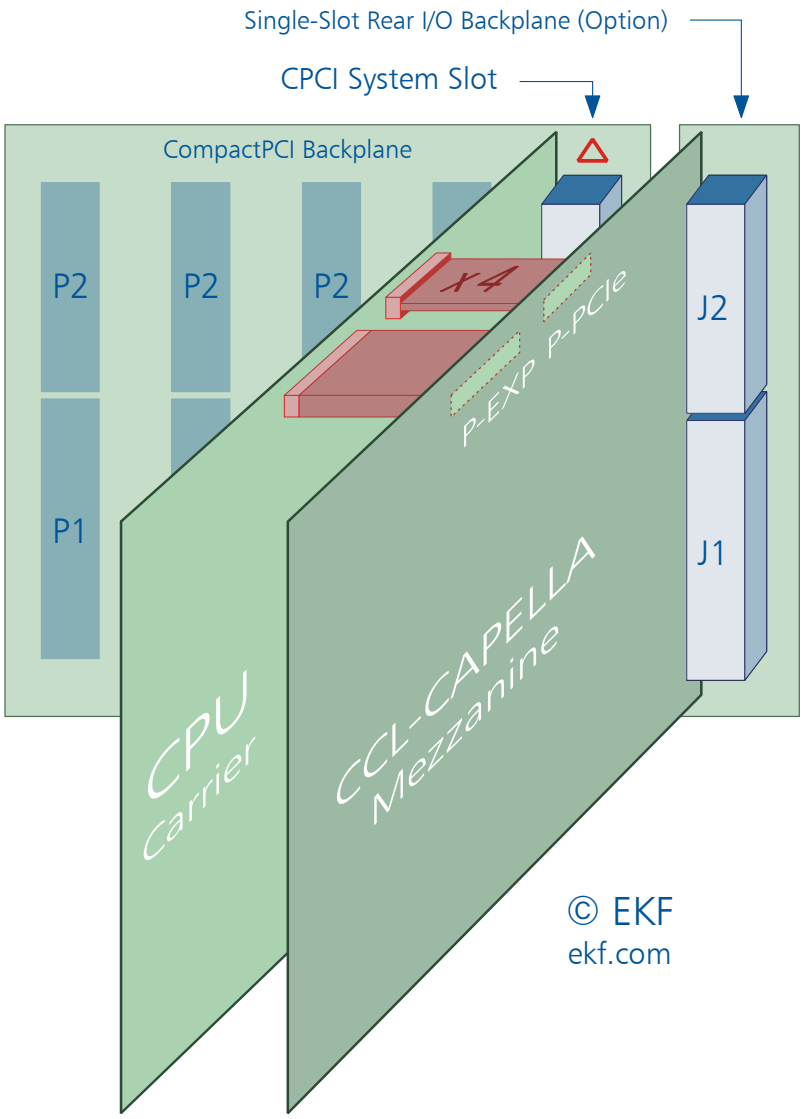
The CCL-CAPELLA communicates by means of two bottom mount expansion connectors with the host CPU: P-PCIE (PCI Express x 4), and P-EXP (multi-function I/F such as LPC, USB, SMB).

The PCI Express interface (connector P-PCIE) is comprised of 4 PCIe lanes, which are derived from the ICH (southbridge chip) on the CPU carrier board. All 4 lanes are routed to the primary port of a 12-port 12-lane PCI Express packet switch, which is the main component of the CCL-CAPELLA.

Connector P-EXP combines several other southbridge data channels: The LPC (Low Pin Count) is a multiplexed ISA bus, e.g. enabling the super-I/O (SIO) controller chip to emulate the legacy I/O interfaces; among these are the classic parallel (printer) and serial (COM) ports. Two USB channels are provided, either for the optional USB SSD headers, or for rear I/O via the J2 connector.

The Trusted Platform Module is an optionally available cryptographic chip, which provides a comprehensive hardware and software solution for safer computing. Conforming to the TPM1.2 standard of the TCG, the TPM is comprised of a 16-bit security controller and additional hardware e.g. to generate 2048 bit RSA keys and true random numbers, thus meeting the highest industry rating for digital security.

The CCL-CAPELLA fits on the top side of the CPU board, which is on the right side when viewing the common front panel. A suitable backplane provides its CPCI slots beginning with the CPU carrier board (CPCI system slot) from right to left. The CPCI system must provide additional mounting space to the right side for the CCL-CAPELLA. In addition, a single slot rear I/O backplane would be needed for rear I/O usage, and a custom specific rear I/O transition module.



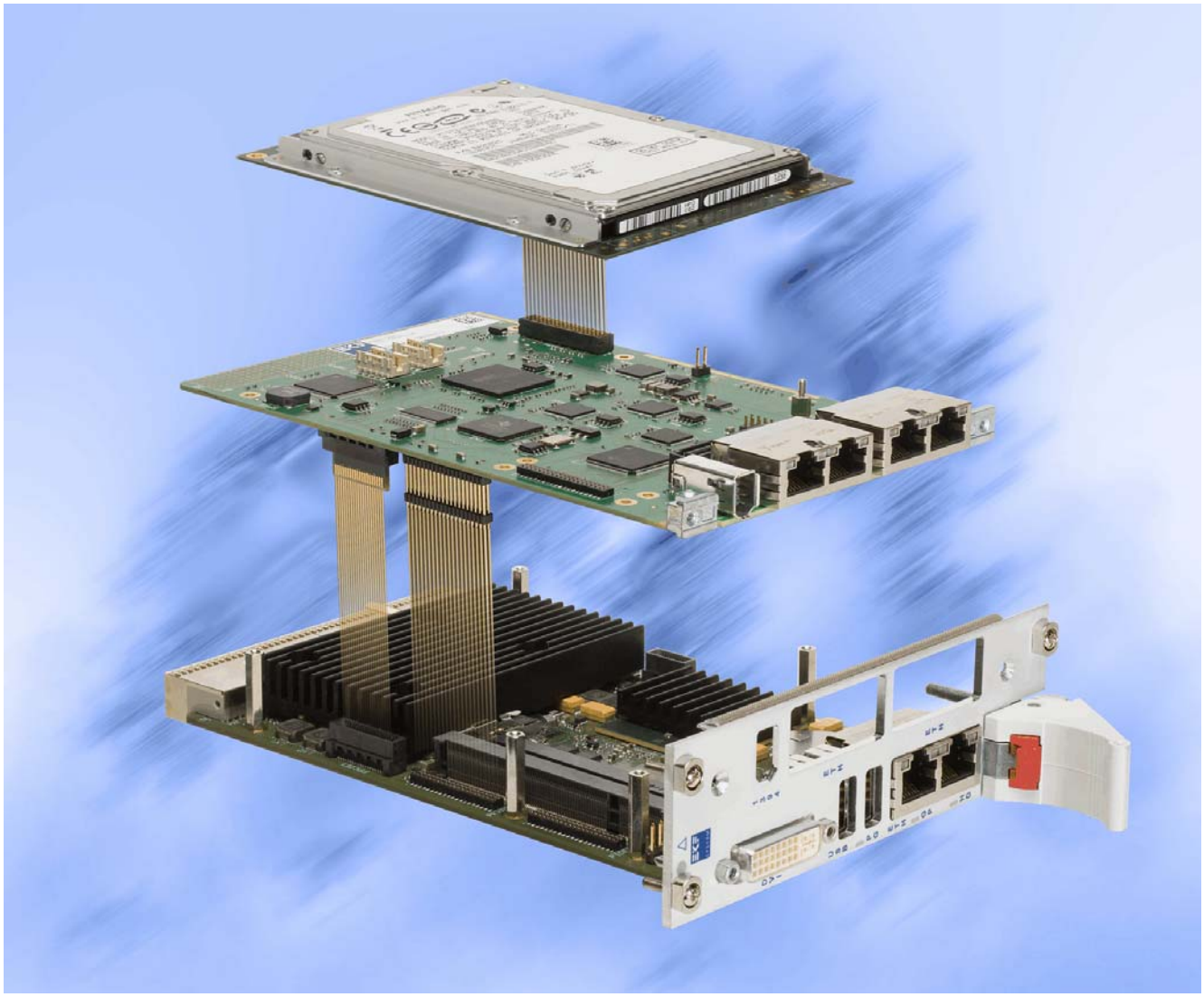
CCL-CAPELLA on Top of the CPU Carrier

As of current, the suitable CPU carrier board for use together with the CCL-CAPELLA mezzanine module is the CCG-RUMBA (successor CCM-BOOGIE available early 2009). The CCL-CAPELLA expansion board mounts on top (at the right side) of the CCG-RUMBA.

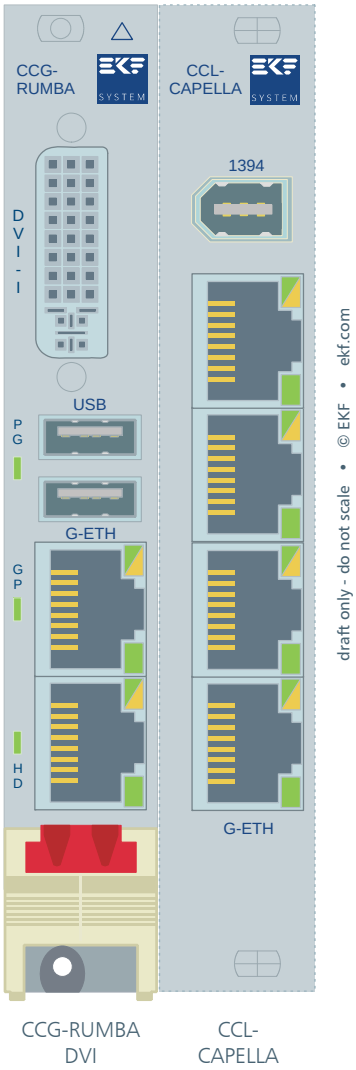
If the CompactPCI backplane is provided with a right aligned system slot, be sure to position the CPU carrier board to the rightmost CPCI slot (and not the CCL-CAPELLA). Consequently, the CCL-CAPELLA then occupies the next card slot to the right, outside of the CPCI backplane, which may be provided with a single slot rear I/O P1/P2 backplane. In order to make use of the rear I/O capability of the CCL-CAPELLA, its optional J1/J2 rear I/O connectors must be stuffed (consider before ordering). This assembly order (right aligned CPCI system slot) is preferred because no CompactPCI slot is lost in a system for the CCL-CAPELLA.

Vice versa, if a CPCI backplane is mandatory with a left aligned system slot, the CCL-CAPELLA must not be equipped with J1/J2 connectors, and occupies a regular CompactPCI slot then. Of course, this assembly solution is not suitable for rear I/O with the CCL-CAPELLA, and a CPCI slot will be lost. With J1/J2 stuffed, a coding key present on J1 would prevent insertion of the CCL-CAPELLA into a CPCI card slot.

The picture below illustrates a typical mezzanine stack, comprised of the CPU carrier board (shared front panel from 4HP to 12HP, individually tailored to customers configuration), the CCL-CAPELLA mezzanine side board, and a SATA storage module (either SSD or hard disk, 1.8-inch or 2.5-inch, dual or single drive, RAID option).



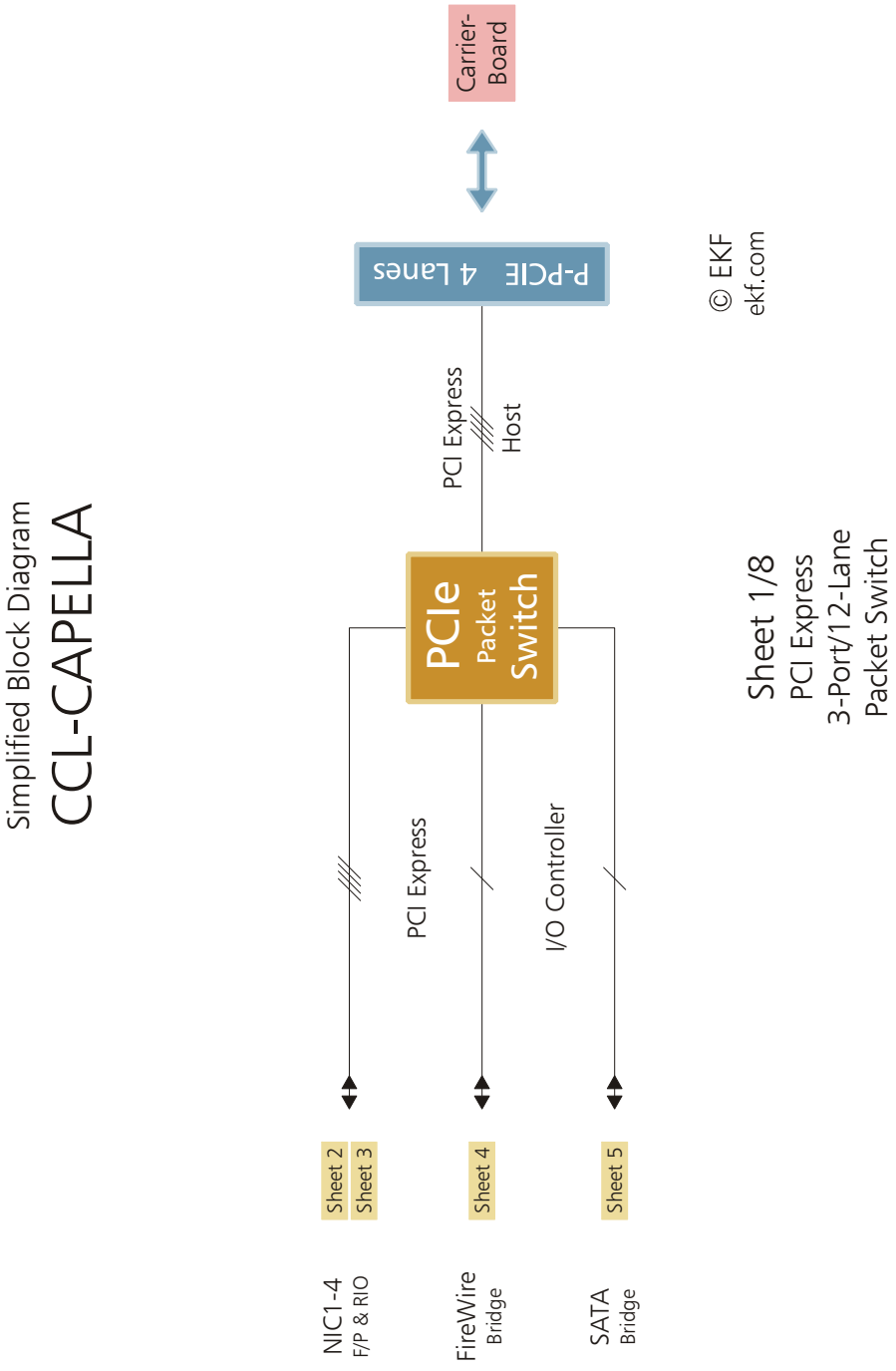
Front Panel

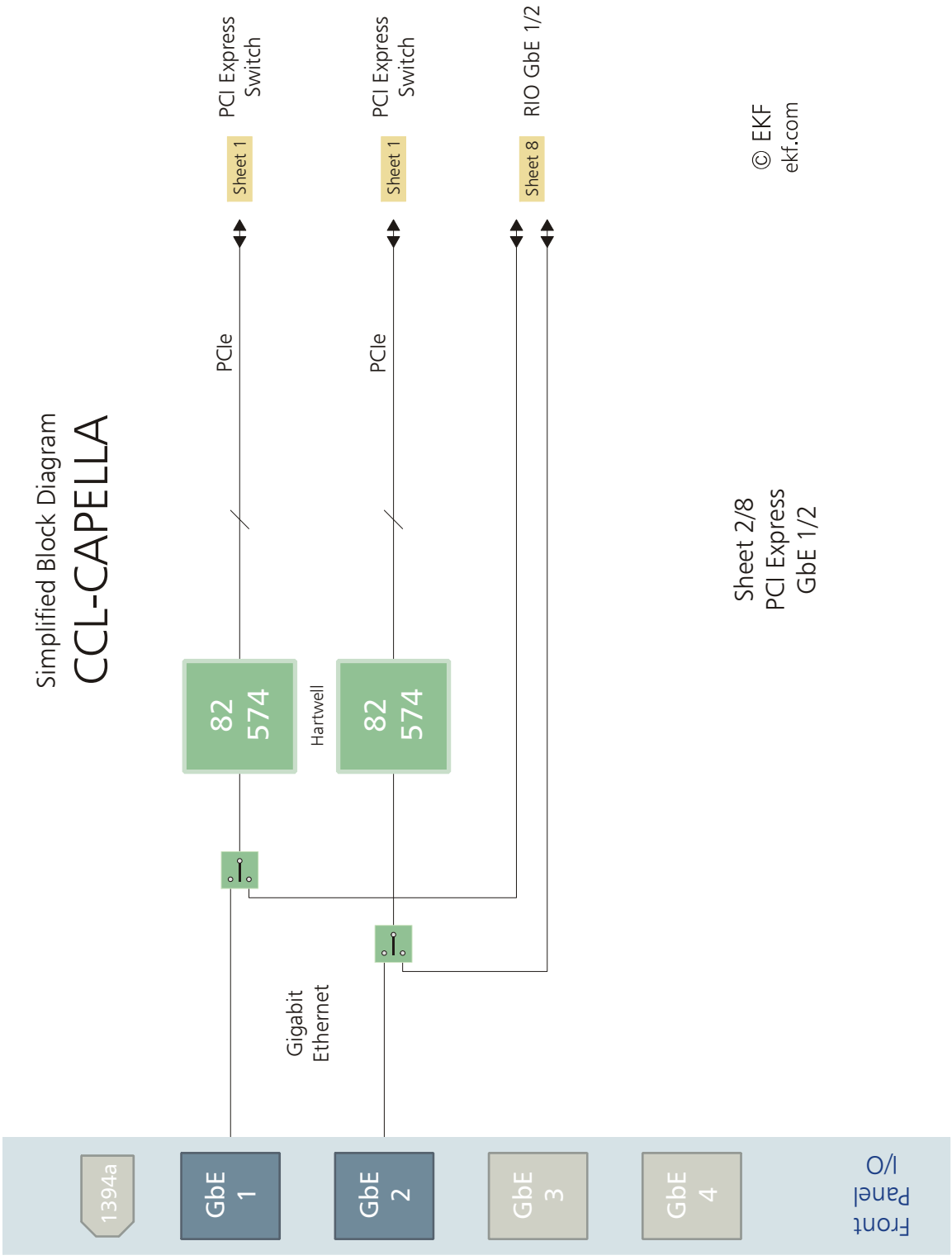


Typically the CCG-RUMBA carrier board CPU and the CCL-CAPELLA share a common 3U/8HP front panel. Not shown in the illustration above are variations of the CCG-RUMBA (e.g. with VGA connector rather than DVI).

There may be reasons for further widening of the front panel (e.g. 12HP width); this would provide additional space e.g. for serial port connectors (CU-series modules). Please discuss your needs for an individual solution with EKF.

Block Diagram CCL-CAPELLA




Simplified Block Diagram
CCL-CAPELLA
PCI Express Switch
Sheet 1
PCI Express Switch
Sheet 1
RIO GbE 1/2
Sheet 8
PCIe
PCIe
82 574
Hartwell
82 574
Gigabit Ethernet
1394a
GbE 1
GbE 2
GbE 3
GbE 4
Front Panel I/O
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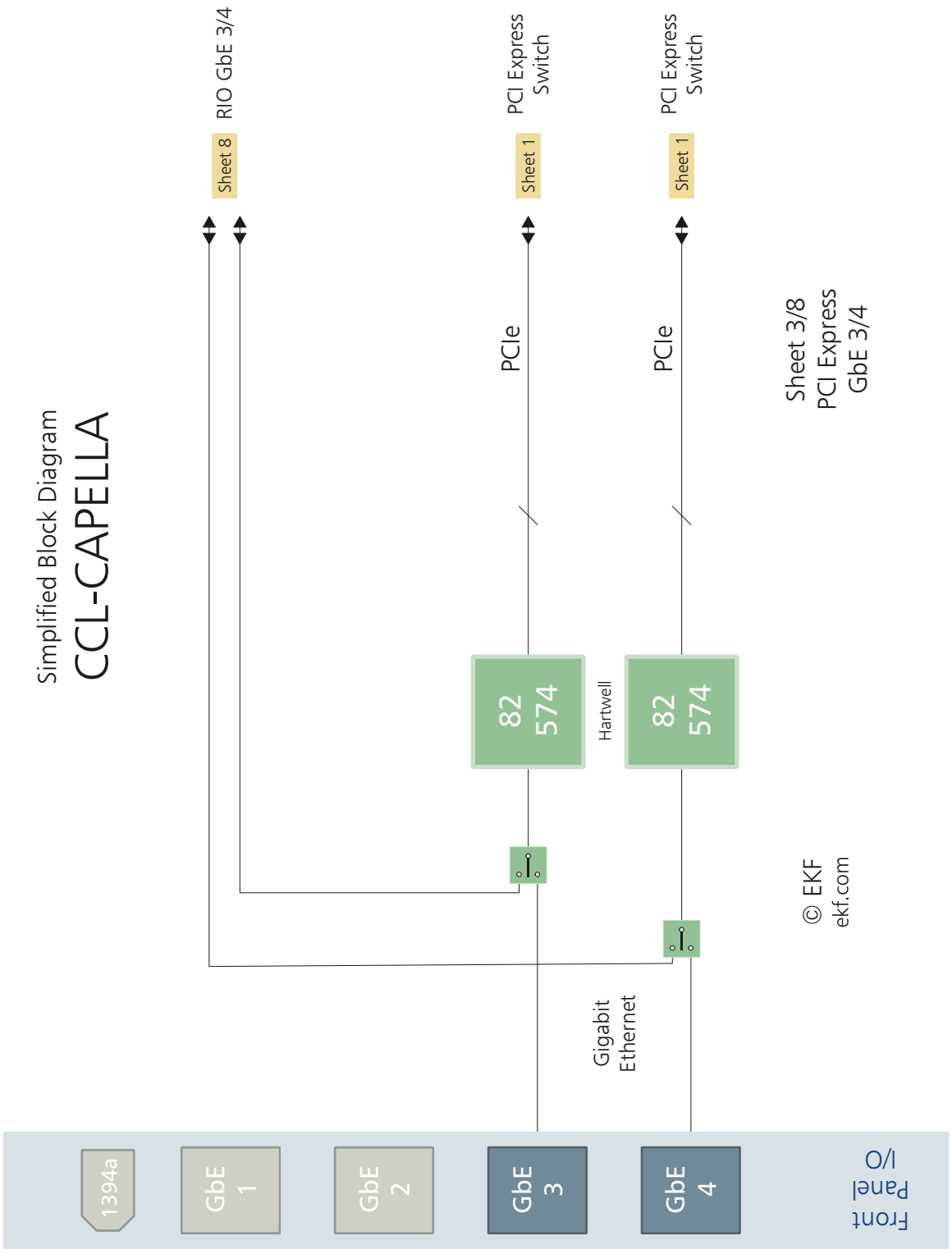
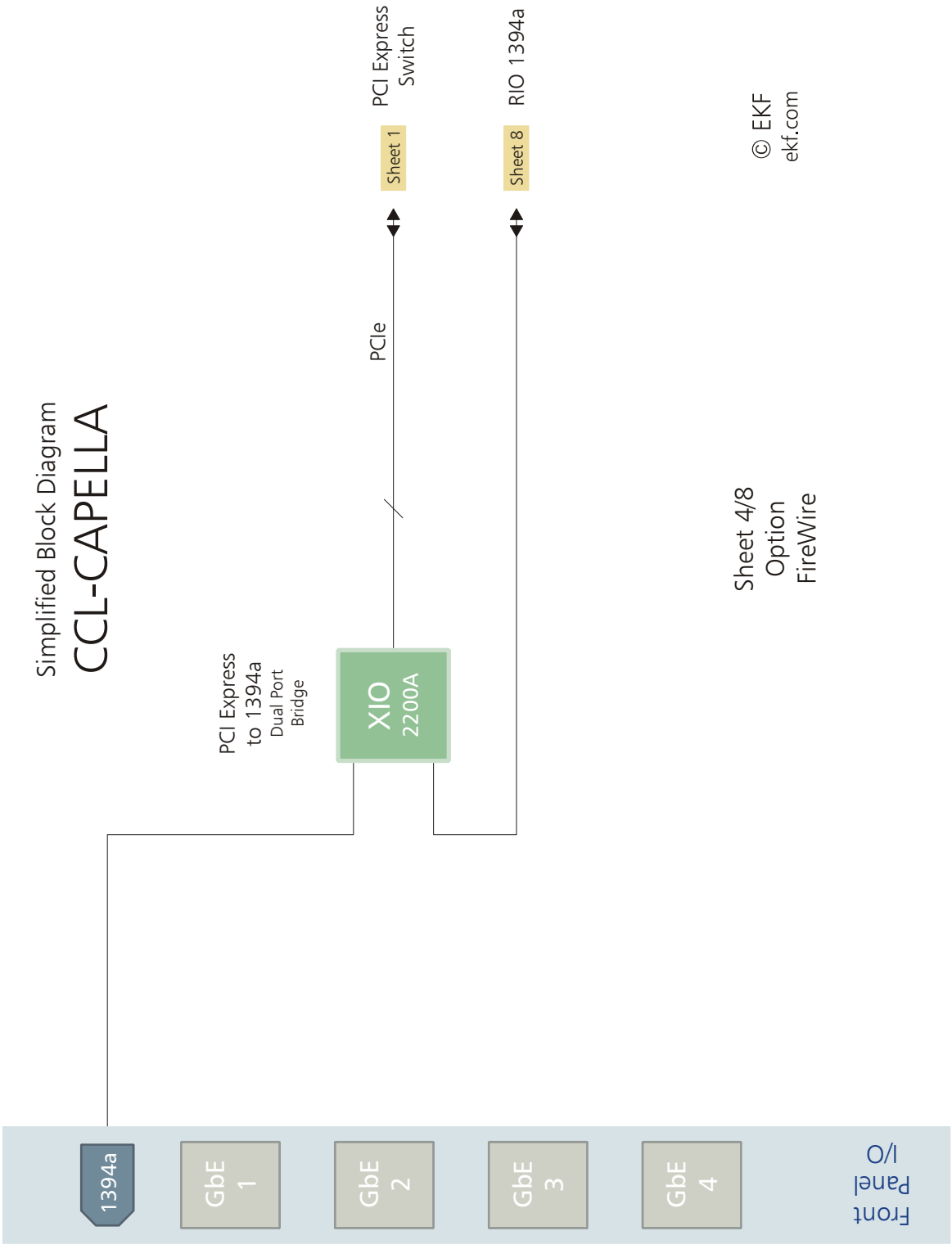
Sheet 2/8
PCI Express
GbE 1/2


Simplified Block Diagram
CCL-CAPELLA
RIO GbE 3/4
Sheet 8
PCI Express Switch
Sheet 1
PCI Express Switch
Sheet 1
PCIe
PCIe
82 574
Hartwell
82 574
Sheet 3/8
PCI Express GbE 3/4
© EKF
ekf.com
Gigabit Ethernet
1394a
GbE 1
GbE 2
GbE 3
GbE 4
Front Panel I/O


Simplified Block Diagram
CCL-CAPELLA
PCI Express
Switch
RIO 1394a
Sheet 1
Sheet 8
PCIe
PCI Express
to 1394a
Dual Port
Bridge
XIO
2200A
Sheet 4/8
Option
FireWire
© EKF
ekf.com
1394a
GbE
1
GbE
2
GbE
3
GbE
4
Front
Panel
I/O

Simplified Block Diagram
CCL-CAPELLA
Sheet 5/8
Option
SATA Storage
P-PCIE
Sheet 1
PCIe
SATA
RAID
Controller
SATA II
3Gbps
SATA/PATA
RAID
Controller
SATA
PATA
P-SATA1
2.5-Inch SATA
Hard Disk Drives
Top & Bottom Mount
C20-SATA
Optional Single/Dual Drive
C20-SATA
Hard Disk Mezzanine Module
P-SATA2
P-SATA3
Optional RIO
SATA Drive(s)
J1
Sheet 8
P-IDE1/2
CompactFlash
cFA
C30-PATA C17-CFA
Optional
C30-PATA (top mount)
C17-CFA (bottom mount)
CompactFlash / SSD Module
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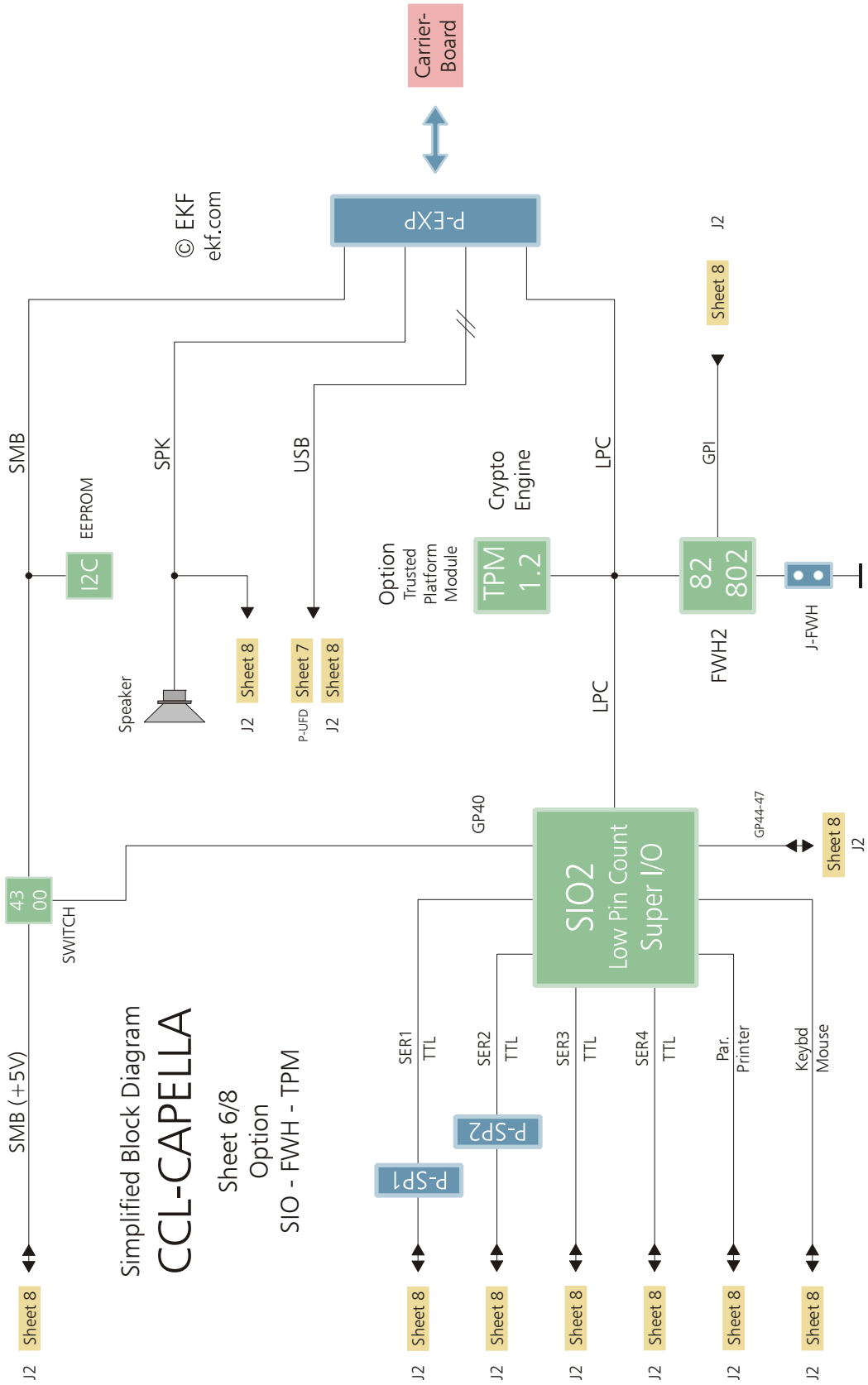
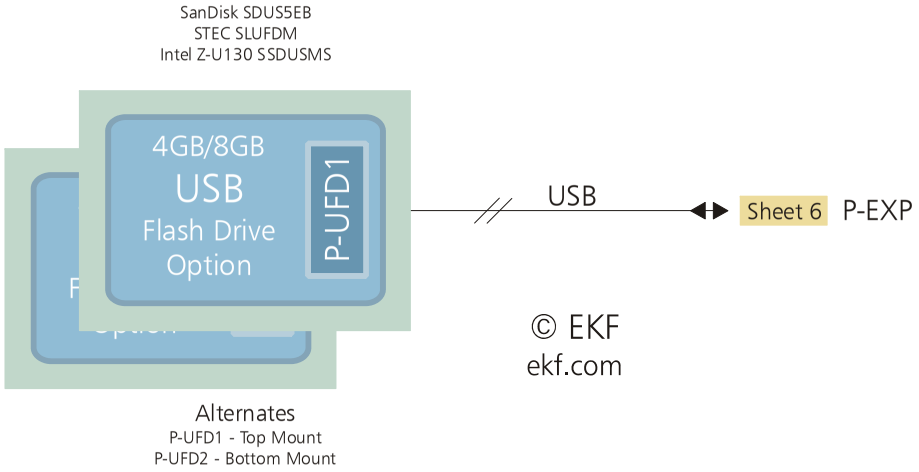
ekf.com


Carrier-Board
P-EXP
© EKF
ekf.com
SMB
SPK
USB
LPC
GPI
J2
Sheet 8
EEPROM
I2C
Speaker
Sheet 8
J2
Sheet 7
P-UFD
Sheet 8
J2
Option
Trusted
Platform
Module
TPM
1.2
Crypto
Engine
82
802
FWH2
J-FWH
LPC
GP40
GP44-47
Sheet 8
J2
43
00
SWITCH
SIO2
Low Pin Count
Super I/O
SMB (+5V)
Simplified Block Diagram
CCL-CAPELLA
Sheet 6/8
Option
SIO - FWH - TPM
SER1
TTL
SER2
TTL
SER3
TTL
SER4
TTL
Par.
Printer
Keybd
Mouse
P-SP1
P-SP2
Sheet 8
J2

Simplified Block Diagram

CCL-CAPELLA

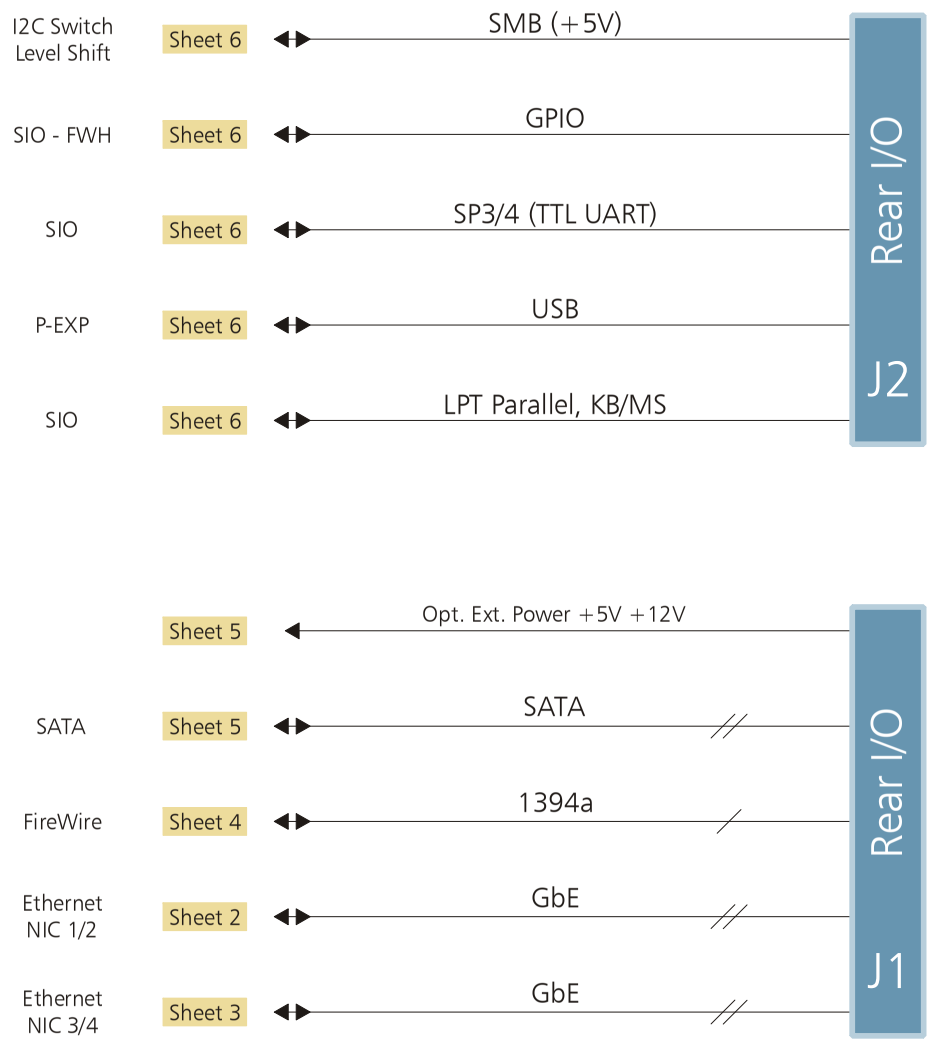
Sheet 7/8
USB Flash Drive



Simplified Block Diagram

CCL-CAPELLA

Sheet 8/8
J1 - J2
Rear I/O
Option



Top View Component Assembly CCL-CAPELLA

Front Panel Connectors

FIW1	1394a FireWire receptacle, PHY port 1
GbE 1-4	RJ45 Gigabit Ethernet Jacks (port 1 = top)

On-Board Connectors

P-IDE1	PATA socket (top mount), suitable for C30-PATA 1.8-inch HDD/SSD module
P-IDE2	PATA socket (bottom mount), suitable for C17-CFA CompactFlash module
P-SATA1	Microspeed female connector, for top mount attachment of a C20-SATA mezzanine module, equipped with either one or two SATA drives 2.5-inch (RAID option with 2 drives)
P-SATA2 P-SATA3	Vertical latched SATA headers, 7-position, stuffing option (exclusive to P-SATA1, and in addition to J1 rear I/O option)
P-SP1 [1] P-SP2	Pin headers 10-lead 2.00mm, provide TTL level serial COM port signals (CU-series modules)
P-UFD1 [2]	Socket (top mount) 10-lead 2.00mm pitch, for low profile USB SSD (Solid State Drive)
P-UFD2 [2]	Socket (bottom mount) 10-lead 2.00mm pitch, for low profile USB SSD (Solid State Drive)

[1] Due to a primary SIO which may be present on the CPU board itself, the BIOS may assign COM port numbers different from COM3/COM4 to these interface lines on the CCL-CAPELLA, e.g. COM4/COM5.

[2] USB channel shared (stuffing option) with J2 for rear I/O

Please note:

Not all of the connectors or other elements listed above may be present or functional on your actual CCL-CAPELLA board. Assembly of these connectors is highly custom specific. Discuss your needs (target application) with EKF before ordering, for an optimum board configuration.

Jumpers

J-FWH [1]	Jumper 2.54mm, determines if the optional on-board firmware hub is acting as boot BIOS (jumper set) or as secondary BIOS (jumper removed = default).
J-RES [1]	Jumper 2.54mm, allows to force a CPU debug reset on the CCG-RUMBA CPU carrier board

[1] Not all of these jumpers may be present or functional on your actual CCL-CAPELLA board. Assembly of these jumpers is highly custom specific. Discuss your needs with EKF before ordering.

Inter-Board Connectors

P-EXP	Dual row socket, available from bottom of the CCL-CAPELLA PCB, matching with the corresponding socket on the CPU carrier board, connected through a board stacker, comprising of: • LPC Low Pin Count interface • HD Audio (Azalia) • 2 x USB • SMB, Speaker, Reset
P-PCIE	High speed socket edge card connector, available from bottom of the CCL-CAPELLA PCB, matching with the corresponding socket on the CPU carrier board, connected through a high speed strip line PCB (C22), comprising of: • Host CPU (ICH8, ICH9) PCI Express (PCIe) x 4 interface

Rear I/O Connectors

J1 [2]	2.00mm brown keyed Hard Metric female connector, signal groups Gigabit Ethernet rear I/O, SATA rear I/O option
J2 [2]	2.00mm Hard Metric female connector, signal groups GPIO, parallel port, serial ports (TTL-level signals), USB, SMB (+5V), speaker

[2] J1/J2 are optional

Please note:

Not all of the connectors or other elements listed above may be present or functional on your actual CCL-CAPELLA board. Assembly of these connectors is highly custom specific. Discuss your needs (target application) with EKF before ordering, for an optimum board configuration.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Technical Reference - Connectors

Caution

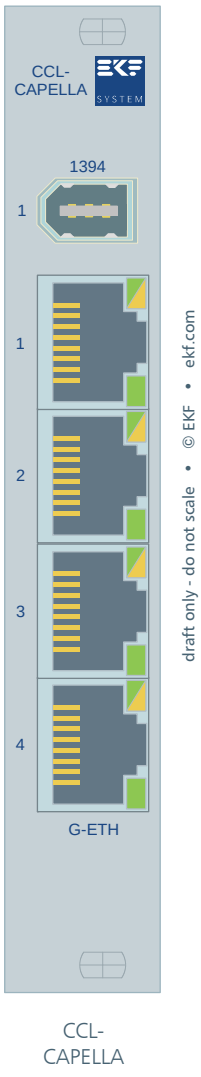
Some of the connectors may provide operating voltage (e.g. +12V, +5V and +3.3V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Please Note

The CCL-CAPELLA mezzanine module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the CCL-CAPELLA board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order within the groups 'front panel connectors', 'on-board connectors', 'inter-board connectors', and 'rear I/O connectors').

Front Panel Connectors

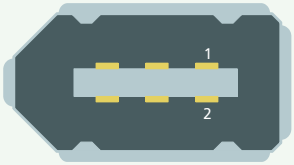
As of current, the suitable CPU carrier board for use together with the CCL-CAPELLA mezzanine module is the CCG-RUMBA. The CCL-CAPELLA side board mounts on top (at the right side) of the CCG-RUMBA. By default, the CCL-CAPELLA shares an 8HP (~40.6mm) front panel with the CPU carrier board. Further more, custom specific front panel options are available on request. Shown below is the basic variant of the CCL-CAPELLA (illustration w/o CCG-RUMBA front panel).



CCL-
CAPELLA

1394 FireWire Connector

The CCL-CAPELLA is equipped with an integrated PCIe to PCI bridge and 1394a OHCI compliant LLC/PHY (XIO2200A). Both cable ports are suitable for data transfer rates of 100Mbps, 200Mbps and 400Mbps according to IEEE1394a-2000. One FireWire port is available directly via the accompanying front panel connector, while the the other is reserved for rear I/O usage across J1.

1394a FireWire Receptacle • 270.30.06.1		
 1394a FireWire Receptacle © EKF • ekf.com • 270.30.06.1	1	+12V/0.5A Bus Power [1]
	2	GND
	3	TP B-
	4	TP B+
	5	TP A-
	6	TP A+

[1] protected by PolySwitch resettable fuse 0.5A, sourced from +12V_CR (carrier board) and +12V_EXT (rear I/O optional connector J1), whatever voltage is higher

The cable port bus power (+12V nominal) on the front panel FireWire receptacle is present if sourced across either

- the rear I/O optional connector J1 with attached power supply (+12V_EXT pin)
- the inter-board connector P-EXP pin 40
- the rear I/O FireWire receptacle (if present e.g. by means of a rear I/O transition module), when a self-powered 1394 device is attached to it

Cable power to the front panel receptacle is fused by a 0.5A PolySwitch (self resettable fuse). Due to a reasonable voltage drop across Schottky diodes in the 12V power lines, the actual bus power voltage may be as low as <11.5V. There may come up a situation where 1394 cable power from the CCL-CAPELLA is not supported: If neither the CompactPCI CPU carrier board is supplied with +12V, nor the CCL-CAPELLA rear I/O J1 connector. This would be not a problem however with a self powered 1394 device attached. EKF CPCI CPU boards are typically designed +12V free for optimum reliability, so there would be no need for a +12V power rail with respect to the CPU carrier card only.

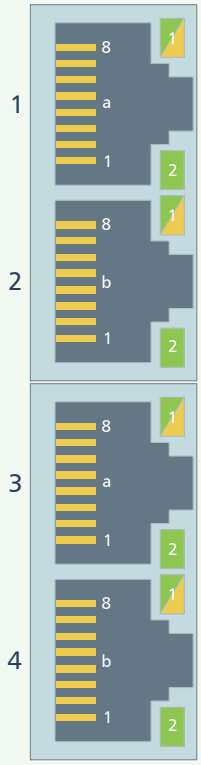
A unique MAC address is assigned to the 1394 controller, similar to the Ethernet ports.

Typical operating systems provide software drivers for TIs FireWire components. If required, e.g. for GPIO programming, the XIO2200A data manual can be obtained from the www.ti.com website.

The FireWire communications path is available as an option. Your actual CCL-CAPELLA may not provide these components.

RJ45 Gigabit Ethernet Jacks

ETH Gigabit Ethernet • 270.02.08.5 2 x Dual RJ45 Jacks



Upper dual-colour LEDs (1):
yellow=1Gbit/s green=100Mbit/s off=10Mbit/s

Lower green LEDs (2):
on=link established blinking=activity (data)

1	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-
2	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-
3	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-
4	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-

The CCL-CAPELLA is equipped with up to four 82574L Gigabit Ethernet controllers for fully concurrent operation. A unique MAC address is individually assigned to each networking controller. For the operating system, the CCL-CAPELLA hence appears as four separate Ethernet NICs.

Each RJ45 jack is provided with a set of status LEDs. The upper LEDs (1) signal the link speed, while the lower LEDs (2) indicate the port activity.

The CCL-CAPELLA allows for front panel access networking, or rear I/O usage. Therefore each Ethernet port is provided with an analog signal switch (octal SPDT style), for either front panel routing (default after system reset), or rear I/O wiring via J1.

Each analog signal switch is controlled (BIOS or customer software) by means of a dedicated general purpose output of the PES12T3 PCI Express package switch. Assignment is as follows:

PES12T3 GPIO Usage		Front Panel Jack	Rear I/O J1
GPIO-02 GbE 1	High	√	
	Low		√
GPIO-03 GbE 2	High	√	
	Low		√
GPIO-04 GbE 3	High	√	
	Low		√
GPIO-05 GbE 4	High	√	
	Low		√

Following a system reset (e.g. as result of the power up cycle), above GPIOs are configured as inputs, with a pull-up resistor. Thus the analog signal switches receive a high voltage on their switching input as long as the GPIOs are not contrary initialized or programmed. The default status immediately after reset therefore is that all Gigabit Ethernet ports are available via the front panel jacks. This may be overridden by BIOS settings. Available as a customer specific stuffing option, the CCL-CAPELLA can be configured for front panel or rear I/O access following a permanent scheme.

The status LEDs within the front panel jacks remain in operation, regardless whether rear I/O Ethernet usage was chosen.

Another two GPIOs are engaged to control the shutdown inputs of the 3rd and 4th 82574 controller, in order to save power if these ports are not in use:

PES12T3 GPIO Usage		NIC Active	NIC Shutdown
GPIO-06 82547 (NIC 3)	High	√	
	Low		√
GPIO-11 82547 (NIC 4)	High	√	
	Low		√

Again, the default state is high (NICs powered up), and a permanent scheme can be provided as customer specific stuffing option.

The CCL-CAPELLA may be equipped with less than 4 Ethernet controllers, as a customer specific option, for cost reduction and power saving effects.

On-Board Connectors

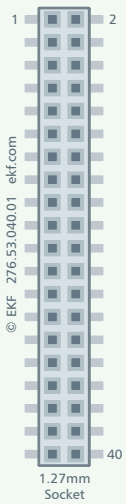
The CCL-CAPELLA can be equipped with several on-board connectors. Some of these connectors are available as an option only or exclusive to each other, and therefore may not be functional or even present on your actual board.

Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering, so that the optimum board configuration for your application will be chosen.

P-IDE1 P-IDE2

The CCL-CAPELLA is optionally provided with sockets for a CompactFlash mezzanine module, or a 1.8-inch hard disk mezzanine module. P-IDE1 is situated on top of the CCL-CAPELLA, while P-IDE2 is bottom mount. Both sockets are wired to the JMB363 controller, which acts as PATA/IDE host controller. Suitable mezzanine modules for P-IDE1/2 are the C17-CFA CompactFlash adapter, or the C30-PATA 1.8-inch HDD carrier board. If both sockets are in use concurrently, attached devices must be configured as IDE master and slave.

P-IDE1 / P-IDE2 CompactFlash/IDE Expansion Interface 1.27mm Socket 2 x 20 (276.53.040.01)



top view pin numbering order (P-IDE1)

IDE_RESET#	1	2	GND
IDE0_DD07	3	4	IDE0_DD08
IDE0_DD06	5	6	IDE0_DD09
IDE0_DD05	7	8	IDE0_DD10
IDE0_DD04	9	10	IDE0_DD11
IDE0_DD03	11	12	IDE0_DD12
IDE0_DD02	13	14	IDE0_DD13
IDE0_DD01	15	16	IDE0_DD14
IDE0_DD00	17	18	IDE0_DD15
GND	19	20	+3.3V_CR *
IDE0_DMARQ	21	22	+3.3V_CR *
IDE0_DIOW#	23	24	GND
IDE0_DIOR#	25	26	GND
IDE0_IORDY	27	28	+5V_CR *
IDE0_DMACK#	29	30	+5V_CR *
IDE0_INTRQ	31	32	GND
IDE0_DA1	33	34	IDE0_CBLID#
IDE0_DA0	35	36	IDE0_DA2
IDE0_CS0#	37	38	IDE0_CS1#
IDE0_ACT#	39	40	GND

* switched power supply lines from CPU carrier board according to Sx state

P-IDE1 suitable for C10-CFA/C30-PATA module (top mount)
P-IDE2 suitable for C17-CFA module (bottom mount)

P-SATA1

The CCL-CAPELLA can be provided with a high speed mezzanine connector for attachment of the C20-SATA hard disk drive module. TX/RX designation of signals is with respect to the on-board SATA controller. The C20-SATA can be equipped with up to two drives (top and bottom mount), and hence is suitable for RAID Level 0/1 operation.

By default, only a single supply voltage (+5V_SATA) is wired to P-SATA1, since popular 2.5-inch SATA hard disk drives do not require +3.3V and/or +12V, as of current. However, these voltages can be supplied as a stuffing option.

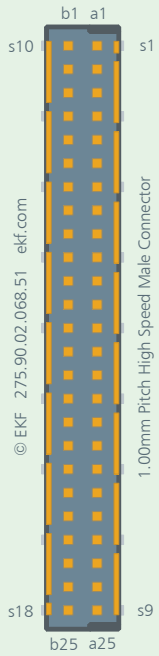
By default, the supply voltages on the P-SATA1 connector are derived from the CPU carrier board. As an alternative, SATA hard disk power could be attached externally, across the rear I/O connector J1 (stuffing option).

Usage of P-SATA1 is exclusive to the P-SATA2/3 headers - discuss your actual needs with sales@ekf.de before ordering. Mixed stuffing of P-SATA1 (single channel SATA operation across P-SATA1) and either one of P-SATA2 or P-SATA3 is also an option. In addition, one or both SATA ports are also available for rear I/O across J1, as further alternative.

The JMB363 is a very popular SATA controller, which allows for several operating modes, including RAID 0, 1, 0+1. Drivers can be downloaded for Windows (WHQL certified) or Linux from ftp://driver.jmicron.com.tw, or alternate driver download portals such as www.pctweaker.net/category/treiber/chipsatz-treiber/jmicron or www.x-drivers.com/component/option,com_remository/func,select/id,4626/.

C20-SATA

P-SATA1 SATA Expansion Interface
1.00mm Pitch Male Connector 2mm Height (275.90.02.068.51)



GND	b1	a1	GND
	b2	a2	SATA0_TXP
	b3	a3	SATA0_TXN
GND	b4	a4	GND
	b5	a5	SATA0_RXN
	b6	a6	SATA0_RXP
GND	b7	a7	GND
	b8	a8	SATA1_TXP
	b9	a9	SATA1_TXN
GND	b10	a10	GND
	b11	a11	SATA1_RXN
	b12	a12	SATA1_RXP
GND	b13	a13	GND
	b14	a14	
	b15	a15	
GND	b16	a16	GND
	b17	a17	
	b18	a18	
	b19	a19	
	b20	a20	
	b21	a21	
+5V_SATA	b22	a22	*+3.3V_SATA*
+5V_SATA	b23	a23	*+3.3V_SATA*
	b24	a24	
	b25	a25	*+12V_SATA*

Notes:

- +3.3V_SATA is not connected by default - can be tied to either +3.3V_CR or +3.3V_EXT as stuffing option
- +5V_SATA by default is connected to +5V_CR across 1.5A PolySwitch resettable fuse - can be tied to +5V_EXT as stuffing option
- +12V_SATA is not connected by default - can be tied to either +12V_CR or +12V_EXT as stuffing option
- All sx pins (shield) are tied to GND
- All TX/RX designations with respect to SATA controller (TX controller = RX drive, RX controller = TX drive)

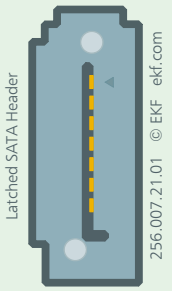
C20-SATA Top View

C20-SATA Bottom View

P-SATA2 P-SATA3

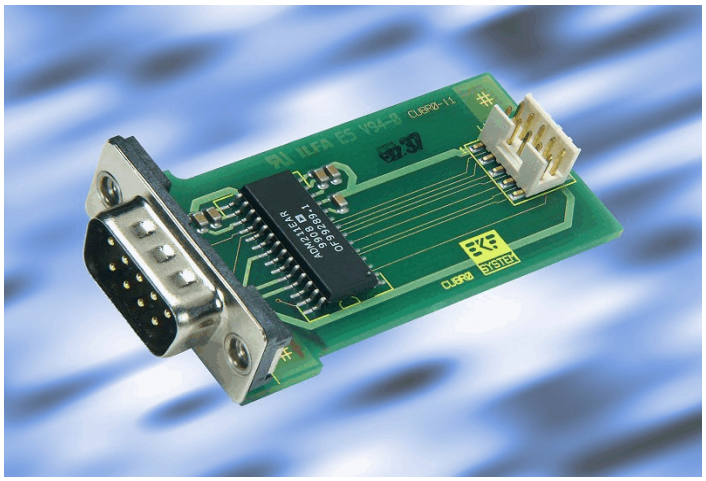
The CCL-CAPELLA can be optionally stuffed with two vertical latched SATA signal headers, for attachment of SATA drives by cable. TX/RX designation of signals is with respect to the SATA controller. P-SATA2 corresponds to the SATA channel 0 of the JMB363 controller, and P-SATA3 is wired to the JMB363 SATA channel 1.

Usage of P-SATA2/3 is exclusive to P-SATA1 - discuss your actual needs with sales@ekf.de before ordering. Mixed stuffing of P-SATA1 (single channel SATA operation across P-SATA1) and either one of P-SATA2 or P-SATA3 is also an option. In addition, one or both SATA ports are also available for rear I/O across J1, as further alternative.

P-SATA2 P-SATA3 #256.007.21.01 Latched Headers		
	1	GND
	2	SATA_TX+
	3	SATA_TX-
	4	GND
	5	SATA_RX-
	6	SATA_RX+
	7	GND

P-SP1 P-SP2

The on-board SIO (Super I/O controller) provides up to four serial interfaces (UART, DOS COM ports). While the serial ports SP3 und SP4 are wired to the optional rear I/O connector J2 only, another two UARTs are available in addition from the optional pin headers P-SP1 and P-SP2 (TTL-level on all signals). P-SP1 and P-SP2 are suitable for attachment of EKF CU-series PHY modules via a micro ribbon flat cable assembly. A PHY module is a transceiver from TTL level signals to a specific symmetric or asymmetric interface standard, e.g. EIA-485 or RS-232E, with or w/o galvanic isolation. Please contact sales@ekf.de for availability of different CU-series modules (inquiries for custom specific PHY or transition modules welcome). Also custom specific front panel design can be done.



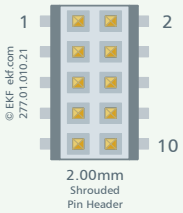
CU-Series PHY Module

Due to another (primary) SIO typically available on the CCG-RUMBA host board, the serial interfaces are not necessarily assigned to COM-1/COM-4 by the operating system. Verify or modify the accompanying CCG-RUMBA or other CPU carrier board BIOS settings for mapping of physical asynchronous serial I/O ports to the logical COM port order.

Alternatively the connector P-SP2 can be used as 5V tolerant programmable I/O (GPIO). Details can be derived from the SCH3114 Super I/O controller data sheet (www.smsc.com).

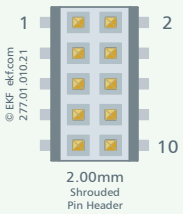
In addition, the serial ports 1 and 2 are also available for rear I/O across J2 (option). In order to avoid signal interference, attach a transceiver module or other circuitry either on-board to P-SP1/2, or on the rear I/O transition module, but not both.

P-SP1 TTL-Level Serial I/O 2.00mm Pin Header 2 x 5 (277.01.010.21)



+5V_SP1 0.5A [1]	1	2	DSR1#
RI1#	3	4	RXD1
TXD1	5	6	DTR1#
RTS1#	7	8	CTS1#
DCD1	9	10	GND

P-SP2 TTL-Level Serial I/O or GPIO 2.00mm Pin Header 2 x 5 (277.01.010.21)

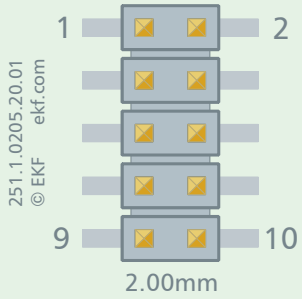


+5V_SP2 0.5A [1]	1	2	DSR2# / GP54
RI2# / GP50	3	4	RXD2 / GP52
TXD2 / GP53	5	6	DTR2# / GP57
RTS2# / GP55	7	8	CTS2# / GP56
DCD2# / GP51	9	10	GND

[1] short circuit protection by a PolySwitch resettable fuse, voltage derived from +5V_CR carrier board switched power well

P-UFD1 P-UFD2

As an option, the CCL-CAPELLA can be equipped with one or two connectors for an industrial style USB Flash disk mezzanine module. The connector is a 2.0mm pitch pin header, suitable for a low profile SSD (Solid-State Drive) 37mm x 26mm. As of current, such modules are available e.g. from STEC, Intel, SanDisk and other manufacturers, up to 8GByte.

P-UFD1 P-UFD2 • 2.00mm Pin Header 2x5 (251.1.0205.20.01) USB Solid-State Drive (Low Profile) 562.20.0004.00 (4GB) Sandisk uSSD 5000 • STec SLUFDM • Intel Z-U130 SSDUSMS				
	+5V_CR	1	2	NC
	USB_D-	3	4	NC
	USB_D+	5	6	NC
	GND	7	8	NC
	Mech. Key	9	10	NC

USB SSD

P-UFD1 and P-UFD2 are provided as a stuffing option only, for a top and/or bottom mount SSD module. The USB ports are derived from the CPU carrier board ICH (southbridge), available via connector P-EXP. If P-UFD1 and/or P-UFD2 are not filled on the CCL-CAPELLA, the associated USB ports are alternatively available for rear I/O across J2.

On-Board Jumpers

Most options on the CCL-CAPELLA are stuffing options, so there are only 2 jumpers which are available for user interaction, J-RES (force reset) and J-FWH2 (select Firmware Hub).

J-RES Reset

Provided as an option, the pin header J-RES can be used for resetting the CPU host board (processor reset) if wired to additional circuitry (e.g. watchdog or manual pushbutton). Tie reset# to GND with an open collector output. While debugging the system, a 2.54mm jumper may be used to force a manual reset.

J-FWH2

Please see description in chapter 'Firmware Hub 2'.

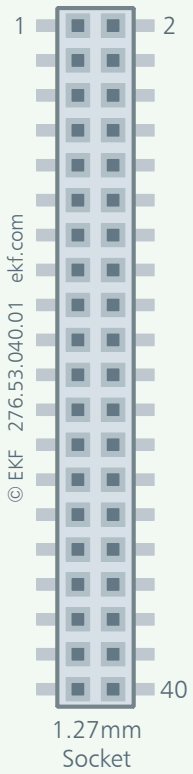
Inter-Board Connectors

The CCL-CAPELLA is equipped with 2 inter-board connectors. These are the P-EXP (LPC and mixed signals), and the P-PCIe (4-Lane PCI Express) connectors. All inter-board connectors are situated at the bottom of the CCL-CAPELLA and establish the data path and power link to the carrier board CPU. As the CCL-CAPELLA comes typically mounted as a unit together with the CCG-RUMBA, there is normally no need for the user to get access to any of the inter-board connectors. They are described here as a reference only and for better understanding of the CCL-CAPELLA.

P-EXP

The inter-board connector P-EXP is mounted on bottom of the CCL-CAPELLA PCB, with its face aligned towards the corresponding connector on the CCG-RUMBA. This allows to attach the CCL-CAPELLA mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards (exactly 4HP distance between PCBs). P-EXP is used to pass the Low Pin Count I/F to the CCL-CAPELLA, besides USB channels and other sideband signals.

P-EXP Expansion Board Interface (LPC/HD-Audio/USB) 1.27mm Socket 2 x 20 (276.53.040.01)



1.27mm Socket

pin orientation shows CPU carrier board top view

GND	1	2	+3.3V_CR *
CLK_33MHZ	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRAME#	9	10	LPC_DRQ#
GND	11	12	+3.3V_CR *
SERIRQ	13	14	PME#
SMI#	15	16	CLK_14MHZ
FWH_ID0	17	18	FWH_INIT#
KBD_RST#	19	20	A20GATE
GND	21	22	+5V_CR *
USB_P2N [1]	23	24	USB_P1N [2]
USB_P2P [1]	25	26	USB_P1P [2]
USB_OC# [3]	27	28	DBRESET#
SMB_CLK	29	30	SMB_DAT
GND	31	32	+5V_CR *
PE Port Cfg Bit 1 [4] *HDA_SDOUT*	33	34	*HDA_SDIN0*
HDA_RST#	35	36	PE Port Cfg Bit 0 [4] *HDA_SYNC*
HDA_BITCLK	37	38	*HDA_SDIN1*
SPEAKER	39	40	+12V_CR

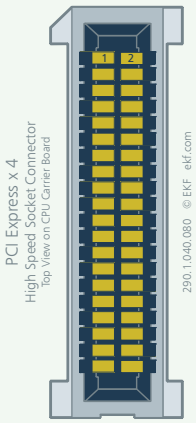
[1] connects to USB Port 6 on CCG-RUMBA
[2] connects to USB Port 5 on CCG-RUMBA
[3] connects to USB_OC56#on CCG-RUMBA
[4] PCI Express port configuration is strapped to 1 link x 4 lanes on the CCL-CAPELLA

* switched power supply lines from CPU carrier board according to Sx state

P-PCIE

The high speed expansion socket P-PCIE is mounted on bottom of the CCL-CAPELLA. This allows to attach the mezzanine companion card on top of the CPU carrier board. A mating strip line spacer PCB (C22-PCIEX2) is used in addition to bridge the gap between the two boards, which results from the horizontal 0.8-inch (20.32mm) card slot pitch.

P-PCIE is organized as 1x4 link (i.e. 4 aggregated PCIe lanes form a link) on the CCL-CAPELLA (refer to hardware strapping signals on P-EXP which indicate the link status to the ICH southbridge on the CPU carrier board).



pin assignment shows CPU carrier board top view (see-trough mezzanine side board PCB)

[1] switched on/off power lines on CPU carrier boards according to S3 state

P-PCIE PCI Express x 4 High Speed Dual Row Socket 0.8mm Pitch 290.1.040.080			
GND	1	2	GND
+5V_CR [1]	3	4	+3.3V_CR [1]
+5V_CR [1]	5	6	+3.3V_CR [1]
GND	7	8	GND
PE_CLKP	9	10	PLTRST#
PE_CLKN	11	12	PE_WAKE#
GND	13	14	GND
PE0_TP	15	16	PE0_RP
PE0_TN	17	18	PE0_RN
GND	19	20	GND
GND	21	22	GND
PE1_TP	23	24	PE1_RP
PE1_TN	25	26	PE1_RN
GND	27	28	GND
PE2_TP	29	30	PE2_RP
PE2_TN	31	32	PE2_RN
GND	33	34	GND
PE3_TP	35	36	PE3_RP
PE3_TN	37	38	PE3_RN
GND	39	40	*+12V_CR* [2]

[1] Supply voltages from carrier board, switched on/off according to sleep state
[2] Stuffing option, no feed through by default

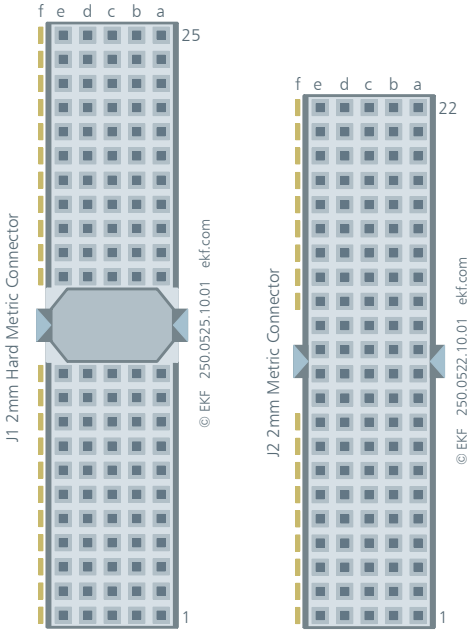
Rear I/O Connectors

J1 J2

As an option, the CCL-CAPELLA can be equipped with the rear I/O connectors J1 and J2. A single slot rear I/O backplane (directly adjoining the CPCI backplane) would be required for handing over the available signal lines to a suitable rear I/O transition module.

Please note, that each Gigabit Ethernet port can be individually switched either to the dedicated front panel jack, or to J1 for rear I/O usage. This is accomplished by analog signal switches under control of 4 GP outputs of the PES12T3 integrated circuit (BIOS settings).

The CCL-CAPELLA must not be plugged into a common CPCI slot in order to avoid damaging the board or other components of the system. A brown key on the J1 connector will prevent the user from erroneously inserting the CCL-CAPELLA into an unsuitable position.



Signal names provided on the J1 and J2 connector tables hereafter are associated with their main function. However, the Super I/O controller allows a number of signals also be used as general purpose I/O. Please consult the SMSC SCH3114 datasheet for details (www.smsc.com).

Please note, that quite a lot of signals are also available either on-board or via front panel. Be sure to have connected any signal only once, in order to avoid interference or even damage.

#J1	A	B	C	D	E
25	+5V_CR		+1.9V	+3.3V_CR	+5V_CR
24	NIC1_MX0+	GND	NIC1_MX1+	NIC1_MX2+	NIC1_MX3+
23	NIC1_MX0-	GND	NIC1_MX1-	NIC1_MX2-	NIC1_MX3-
22	NIC2_MX0+	GND	NIC2_MX1+	NIC2_MX2+	NIC2_MX3+
21	NIC2_MX0-	GND	NIC2_MX1-	NIC2_MX2-	NIC2_MX3-
20	GND	GND	GND	GND	GND
19	NIC3_MX0+	GND	NIC3_MX1+	NIC3_MX2+	NIC3_MX3+
18	NIC3_MX0-	GND	NIC3_MX1-	NIC3_MX2-	NIC3_MX3-
17	GND	GND	GND	GND	GND
16	NIC4_MX0+	GND	NIC4_MX1+	NIC4_MX2+	NIC4_MX3+
15	NIC4_MX0-	GND	NIC4_MX1-	NIC4_MX2-	NIC4_MX3-
14					
13			KEY (BROWN)		
12					
11	SATA0 TX+	GND			
10	SATA0 TX-	GND			
9	+5V_EXT *	+3.3V_EXT *	GND	*-12V_EXT **	+12V_EXT *
8	SATA0 RX-	GND	GND		
7	SATA0 RX+	GND	GND		GND
6	GND	GND	1394_TPA0P 1)		1394_TPA1P
5	SATA1 TX+	GND	1394_TPA0N 1)		1394_TPA1N
4	SATA1 TX-	GND	GND	1394_12V	GND
3	GND	GND	1394_TPB0N 1)		1394_TPB1N
2	SATA1 RX-	GND	1394_TPB0P 1)		1394_TPB1P
1	SATA1 RX+	GND	GND		GND

* optional external supply voltages for C20-SATA mezzanine (Hard Disk)

1) Stuffing option - this FireWire port can be wired either to front panel connector or as rear I/O

Gigabit Ethernet ports are either available on front panel jacks, or for rear I/O across J1. Each individual GbE channel is routed through an analog switch. Direction is controlled by PES12T3 GPIO02 –> NIC1, GPIO03 –> NIC2, GPIO04 –> NIC3 and GPIO05 –> NIC4. A high GPIO signal sets the analog switch for GbE front panel access, a low GPIO signal sets the particular analog switch to rear I/O direction. If rear I/O Ethernet is chosen, additional magnetics must be provided on the rear I/O transition module (connect center tap to +1.9V).

#J2	A	B	C	D	E
22	+5V_CR	+3.3V_CR	RSVD	RSVD	+12V_CR
21	GND	GND	GND	GND	GND
20	SP1_RI#	SP1_CTS#	SP2_RI# / GP50	SP2_CTS# / GP56	RSVD
19	SP1_RXD	GND	SP2_RXD / GP52	GND	FWH_GPI1
18	SP1_DSR#	SP1_DCD#	SP2_DSR# / GP54	SP2_DCD# / GP51	FWH_GPI2
17	SP1_DTR# 3)	GND	SP2_DTR# / GP57	GND	GND
16	SP1_RTS# 3)	SP1_TXD	SP2_RTS# / GP55 3)	SP2_TXD / GP53	DBRESET#
15	RSVD	GND	RSVD	GND	RSVD
14	SP3_RI# / GP13	SP3_CTS# / GP16	SP4_RI# / GP31	SP4_CTS# / GP62	SMB_DAT 1)
13	SP3_RXD / GP10	GND	SP4_RXD / GP64	GND	SMB_CLK 1)
12	SP3_DSR# / GP14	SP3_DCD# / GP12	SP4_DSR# / GP66	SP4_DCD# / GP63	GND
11	SP3_DTR# / GP15	GND	SP4_DTR# / GP34 2)	GND	USB1_D- 4)
10	SP3_RTS# / GP17	SP3_TXD / GP11	SP4_RTS# / GP67 2)	SP4_TXD / GP65	USB1_D+ 4)
9	RSVD	GND	RSVD	GND	GND
8	LPT_SLCT	LPT_PE	LPT_BUSY	SIO_GP47	USB_OC#
7	LPT_ACK#	GND	GND	SIO_GP46	GND
6	LPT_D7	LPT_D6	LPT_D5	SIO_GP45	USB2_D- 4)
5	LPT_D4	GND	LPT_D3	SIO_GP44	USB2_D+ 4)
4	LPT_D2	LPT_D1	LPT_SLCTIN#	SPEAKER	GND
3	LPT_D0	GND	LPT_INIT#	KBDAT	KBCLK
2	LPT_ALF#	LPT_ERROR#	LPT_STROBE#	GND	+5V_CR
1	GND	GND	GND	MSDAT	MSCLK

1) stuffing option: SM Bus signals buffered via LTC4300A-3, voltage level @ +5V_CR
buffer enable input is controlled by GP40 SCH3114 SIO (high=enabled)

2) GP34 may be used to control serial EEPROM A1 (stuffing option)
GP67 may be used to control serial EEPROM WP (stuffing option)

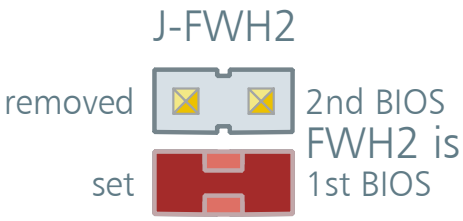
3) These serial port handshake signals may be also in use for power up strapping options of the SCH3114 SIO (10k PU or PD) with no or minor impact on normal operation

4) Stuffing option - USB port(s) may be in use for on-board Solid State Disk(s)

Additional Functions

Firmware Hub 2

The CCL-CAPELLA is optionally provided with a 82802 compatible 8Mbit Flash (Firmware Hub), which can be used either as alternative boot BIOS, as an expansion memory to the CPU board BIOS, or for BIOS retrieval/rescue. The Firmware Hub is connected to the LPC (Low Pin Count) interface. The device ID of a particular FWH determines whether it is detected as BIOS after power on (ID = 0). If stuffed, the jumper J-FWH sets the on-board FWH2 ID to zero (and simultaneously changes the CCG-RUMBA SPI Flash BIOS ID to 1) - hence the system will use the BIOS on the CCL-CAPELLA after power-on.



- jumper removed: system boots from carrier board FWH
- jumper set: system boots from mezzanine board FWH2

A programming tool for the Firmware Hub and latest BIOS releases can be obtained from the EKF website.

SMBus EEPROM

The CCL-CAPELLA is provided with a 24C01 1Kbit I^2C EEPROM, for storing board configuration data. The EEPROM is accessed via the SMBus. If there is need for storing additional customer data, EKF can place an EEPROM instead with custom specific data space, e.g. 24C16.

If required, the SMBus EEPROM A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), and the SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#).

Trusted Platform Module

The CCL-CAPELLA can be optionally equipped with a Trusted Platform Module cryptogCAPELLAhic chip according to the TPM 1.2 specification. The board provides a footprint which is suitable for

- SLB9635 (Infineon www.infineon.com/tpm)
- AT97SC3203 (Atmel www.atmel.com)

and other brands. The TPM chip communicates with the CPU carrier board through the LPC interface. Recent operating systems such as Windows Vista and Linux provide TPM software support.

Typically, TPM chip manufacturers provide the necessary device driver software for integration into special operating systems, along with BIOS drivers. Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 – 3, on the TCG website located at https://www.trustedcomputinggroup.org/. TPM features specific to PC Client platforms are specified in the "TCG PC Client Specific TPM Interface Specification, Version 1.2", also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the "TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2", also available on the TCG web site.

Atmels TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 500 ms and a 1024-bit RSA signature in 100ms. Performance of the SHA-1 accelerator is 50us per 64-byte block. TCG key generation operations will be completed using a proprietary mechanism in less than 1 msec. The TPM is offered to OEM manufacturers as a turnkey solution, including the firmware integrated on the chip.

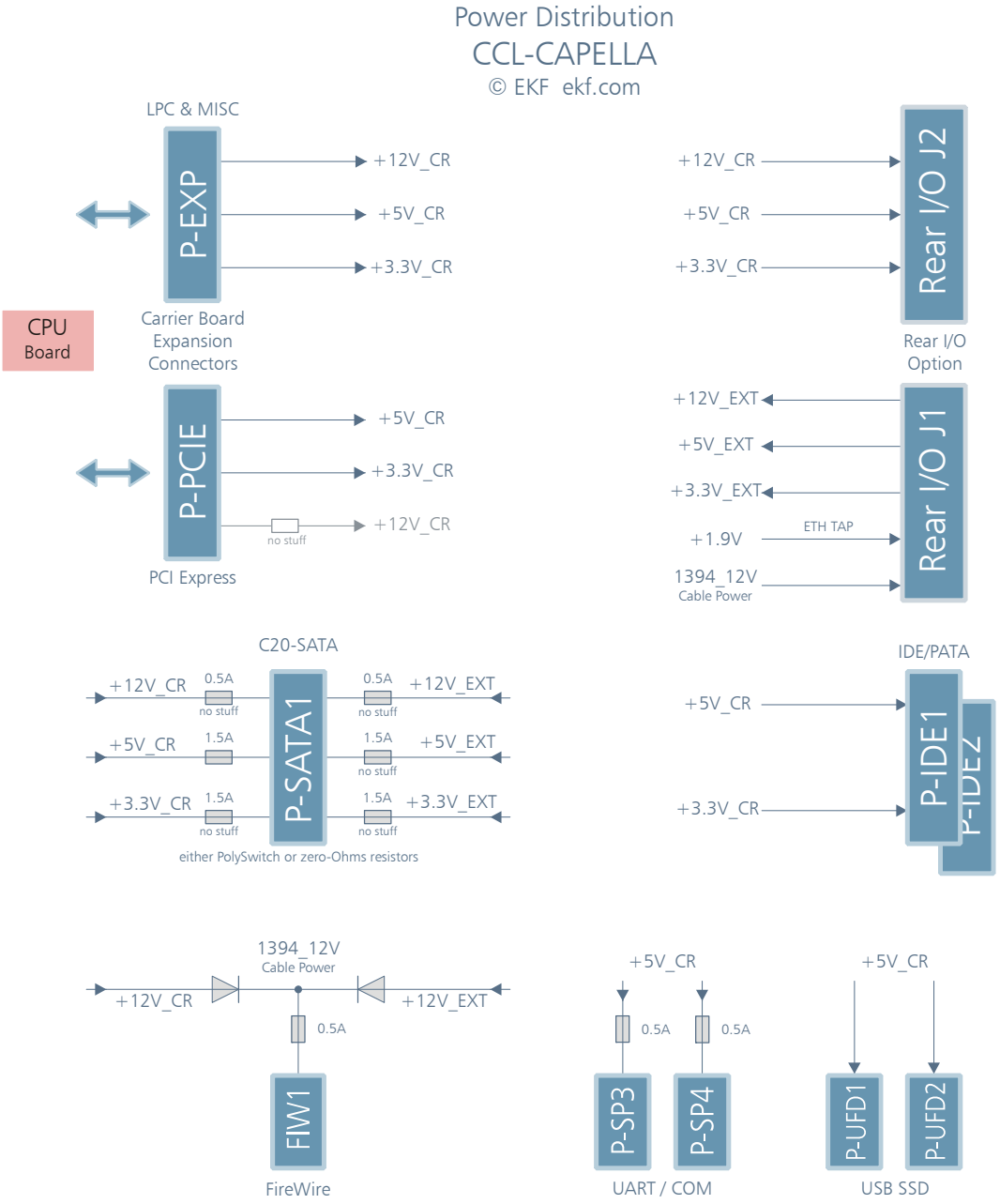
Infineons security controllers have achieved the industry's highest rating for digital security, the Common Criteria EAL 5 high Certificate issued by the German government agency responsible for security in information technology. Infineon provides OEMs with a complete TCG solution that includes all required hardware, software, and management utilities to develop a complete platform security solution.

Power Distribution

The CCL-CAPELLA gets its power from two possible sources: The CPU carrier board supplies +3.3V_CR, +5V_CR, and +12V_CR, which may be switched off according to the current system sleep state. In addition, the rear I/O connector J1 can also be used to deliver alternate power to the SATA drives (+12V_EXT, +5V_EXT, +3.3V_EXT), and to the FireWire front panel connectors (+12V_EXT).

For the C20-SATA hard disk drive mezzanine module, the +5V power source can be selected by a Polyswitch resettable fuse (stuffing option) between +5V_CR and +5V_EXT. Typically, neither +12V nor +3.3V are required for SATA devices, so there should be no need for +12V_CR/+12V_EXT and +3.3V_CR/+3.3V_EXT from this point of view.

The 1394_12V bus power is derived concurrently from either the carrier board +12V_CR, or the J1 +12V_EXT, whatever voltage is higher (back-driving protection by Schottky diodes). No cable power would be required for attachment of self powered 1394 devices.



Schematics

Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact sales@ekf.de for details.

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Industrial Computers Made in Germany

boards. systems. solutions.

EKF Elektronik GmbH
Philipp-Reis-Str. 4
59065 Hamm
Germany

Phone +49 (0)2381/6890-0
Fax +49 (0)2381/6890-90
Internet www.ekf.com
E-Mail info@ekf.com